D45/D46 Block Diagram

Project code: 91.4J001.001--D45
91.4K001.001--D46
PCB P/N : 07248
REVISION : SA

CLK GEN.
ICS9LPRS365YGLFT-GP
3
RTM875T-606-VD-GRT

Mobile CPU
Penryn
4, 5

G7921
20

HOST BUS 667/800/1066MHz@1.05V

DDR2 socket
12,13

DDR2 socket
12,13

800/667MHz

800/667MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CNTIG.00U
6,7,8,9,10,11

X4 DMI 400MHz

C-Link0

PCI-EG

ATI
M82M
VRAMx4 256MB
41~47

LVDS
WXGA/SXGA+ 15"LCD 14

RGB CRT
CRT 13

S-Video
S-Video 13

Headphone Out
MIC In
29
INT.MIC
29
INT.SPKR

Codec
ALC269
29

AZALIA

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
12 USB
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH9M.00U
16,17,18,19

PCI-E/USB 2.0
New card
25
G577
25

PCI-E
USB Cardreader
JMICRO380
26
MS/MS Pro/ MMC/SD
4 in 1
26
1394

PCI-E
LAN
TRL8111C
23
TXFM
24
RJ45
24

PCI-E /USB 2.0
Mini Card
Kedron a/b/g/n
25

PCI-E /USB 2.0
Mini Card
UMTS(3G)
25

RJ11
MODEM
MDC Card
22

LPC BUS

SATA
SATA
SATA
USB0
USB

BlueTooth
22

KBC
Winbond
WPC773
28

SPI I/F
BIOS
4M byte
28

LPC
DEBUG
CONN.
27

HDD
21

CDROM
21

eSATA /USB
22

USB 3 Port
22

CAMERA
14

Touch Pad
27

INT. KB
27

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
TPS51125
34

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC
TPS51124
36

INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D8V_S3(10A)

RT9026
35

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

G9131
35

3D3V_S0	2D5V_S0 (300mA)

APL5912
35

1D8V_S3	1D5V_S0

NB DC/DC
ISL6263A
37

INPUTS	OUTPUTS
DCBATOUT	GFX_CORE

CHARGER
BQ24745
38

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6266A
33

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: D45/D46 | Rev: PD

Date: Friday, March 14, 2008 | Sheet 1 of 47

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

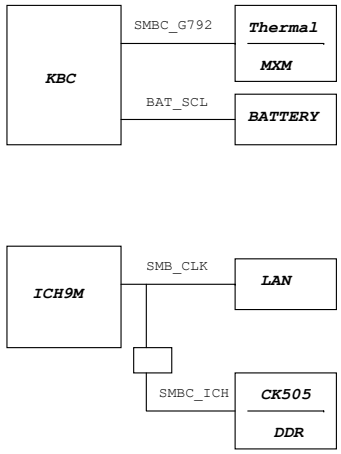
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	Combo(ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

www.vinafix.vn

UMA

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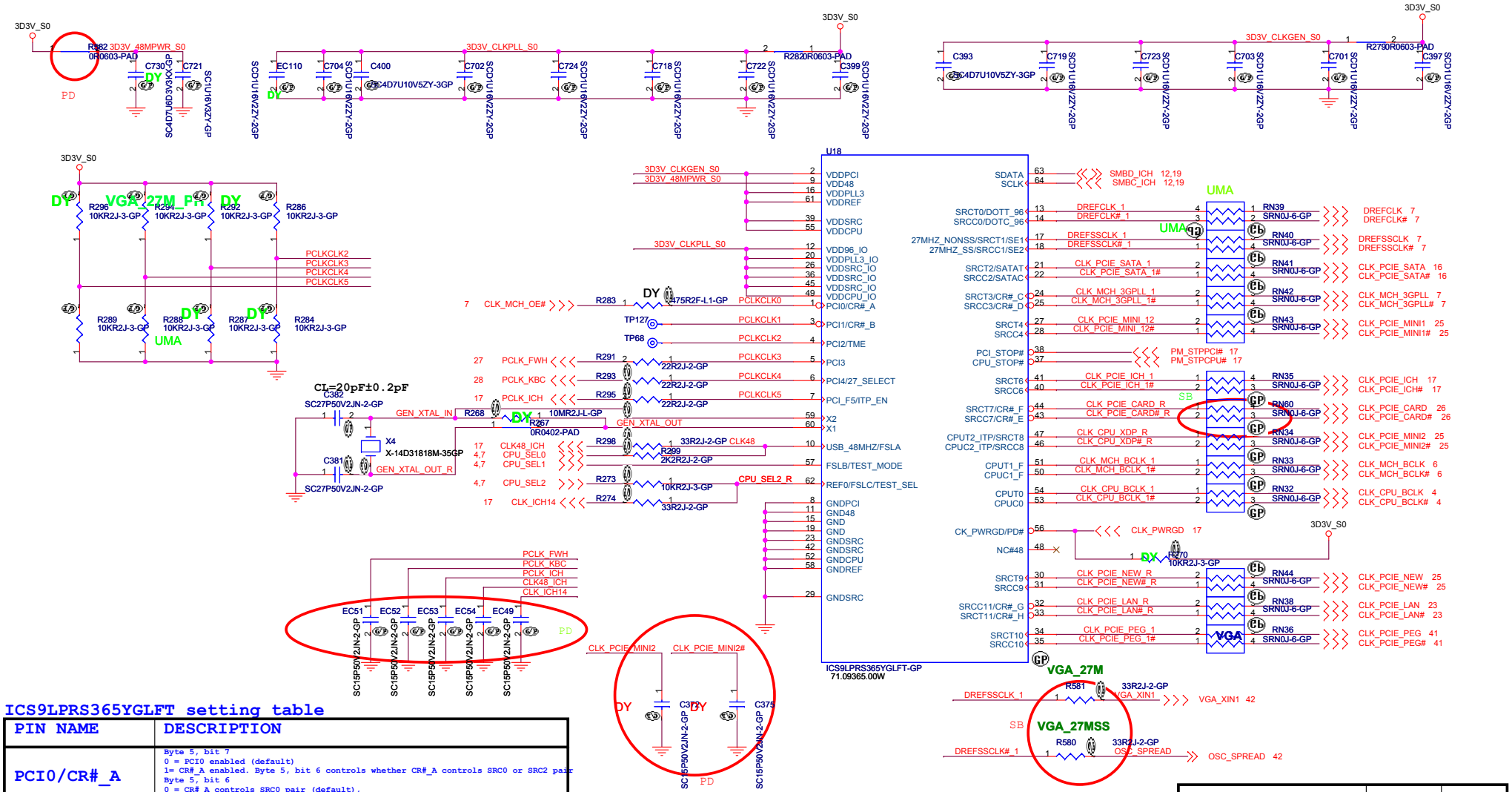
Title: Reference

Size | Document Number: D45/D46 | Rev: PD

Date: Friday, March 14, 2008 Sheet 2 of 47


3D3V_S0
3D3V_48MPWR_S0
3D3V_CLKPLL_S0
3D3V_CLKGEN_S0
U18
ICS9LPRS365YGLFT-GP
71.09365.00W
VDDPCI
VDD48
VDDPLL3
VDDREF
VDDSRC
VDDCPU
VDD96_IO
VDDPLL3_IO
VDDSRC_IO
VDDCPU_IO
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
X2
X1
USB_48MHZ/FSLA
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
GNDPCI
GND48
GND
GNDSRC
GNDCPU
GNDREF
SDATA
SCLK
SRCT0/DOTT_96
SRCC0/DOTC_96
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
SRCT2/SATAT
SRCC2/SATAC
SRCT3/CR#_C
SRCC3/CR#_D
SRCT4
SRCC4
PCI_STOP#
CPU_STOP#
SRCT6
SRCC6
SRCT7/CR#_F
SRCC7/CR#_E
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
CPUT1_F
CPUC1_F
CPUT0
CPUC0
CK_PWRGD/PD#
NC#48
SRCT9
SRCC9
SRCC11/CR#_G
SRCT11/CR#_H
SRCT10
SRCC10
UMA
SB
VGA
VGA_27M
VGA_27MSS
CL=20pF±0.2pF
X4
X-14D31818M-35GP
0R0402-PAD
PD
DY
ICS9LPRS365YGLFT setting table
PIN NAME
DESCRIPTION
PCI0/CR#_A
Byte 5, bit 7
0 = PCI0 enabled (default)
1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair
Byte 5, bit 6
0 = CR#_A controls SRC0 pair (default),
1= CR#_A controls SRC2 pair
PCI1/CR#_B
Byte 5, bit 5
0 = PCI1 enabled (default)
1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair
Byte 5, bit 4
0 = CR#_B controls SRC1 pair (default)
1= CR#_B controls SRC4 pair
PCI2/TME
0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed
PCI3
PCI4/27M_SEL
0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96#
1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN
0 =SRC8/SRC8#
1 = ITP/ITP#
SRCT3/CR#_C
Byte 5, bit 3
0 = SRC3 enabled (default)
1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair
Byte 5, bit 2
0 = CR#_C controls SRC0 pair (default),
1= CR#_C controls SRC2 pair
PIN NAME
DESCRIPTION
SRCC3/CR#_D
Byte 5, bit 1
0 = SRC3 enabled (default)
1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair
Byte 5, bit 0
0 = CR#_D controls SRC1 pair (default)
1= CR#_D controls SRC4 pair
SRCC7/CR#_E
Byte 6, bit 7
0 = SRC7# enabled (default)
1= CR#_F controls SRC6
SRCT7/CR#_F
Byte 6, bit 6
0 = SRC7 enabled (default)
1= CR#_F controls SRC8
SRCC11/CR#_G
Byte 6, bit 5
0 = SRC11# enabled (default)
1= CR#_G controls SRC9
SRCT11/CR#_H
Byte 6, bit 4
0 = SRC11 enabled (default)
1= CR#_H controls SRC10
SEL2 FSC
SEL1 FSB
SEL0 FSA
CPU
FSB
1 0 1 100M X
0 0 1 133M 533M
0 1 1 166M 667M
0 1 0 200M 800M
0 0 0 266M 1067M
UMA
緯創資通
Wistron Corporation
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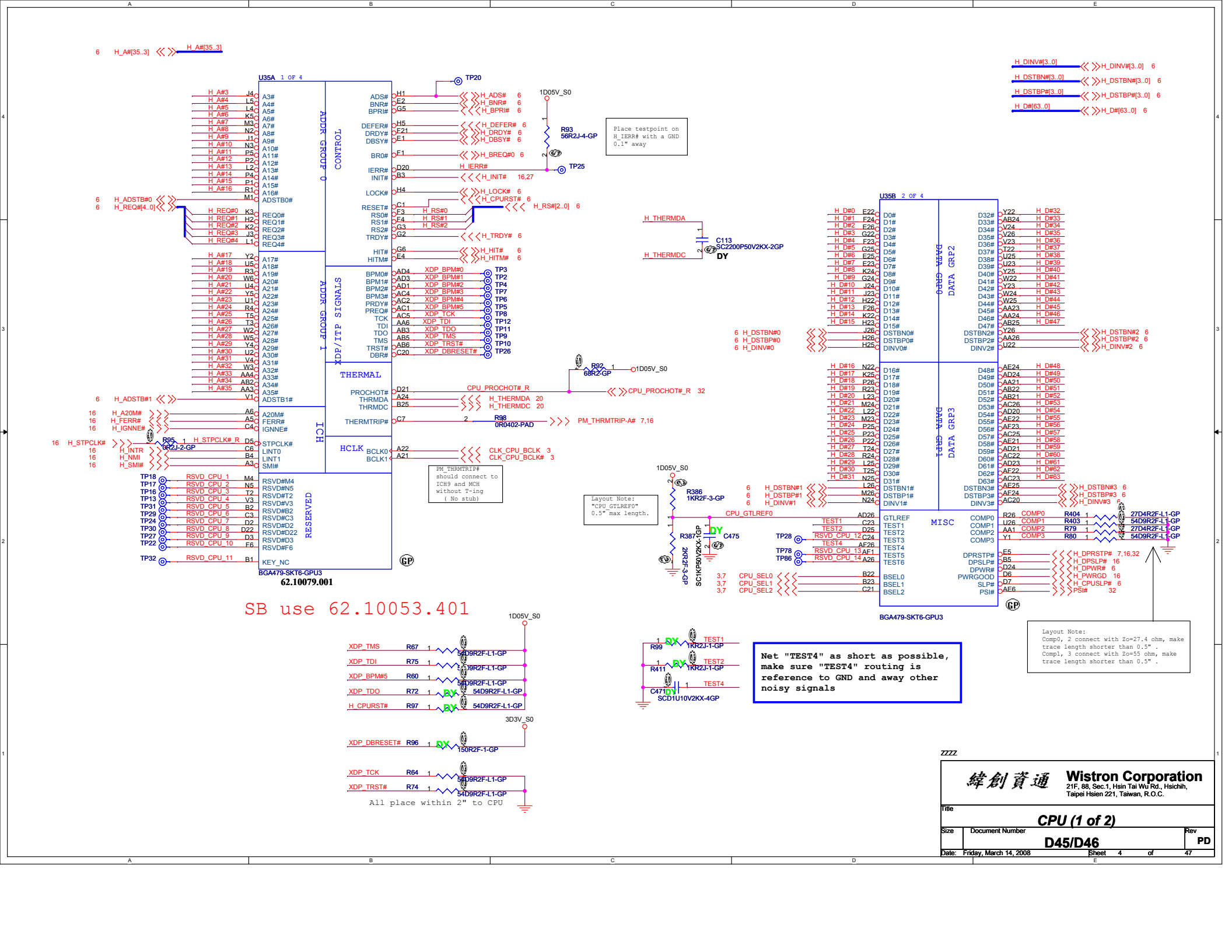
Title
Clock Generator
Size
Document Number
D45/D46
Rev
PD
Date: Tuesday, March 18, 2008
Sheet 3 of 47


U35A 1 OF 4
BGA479-SKT6-GPU3
62.10079.001
U35B 2 OF 4
BGA479-SKT6-GPU3
SB use 62.10053.401
All place within 2" to CPU
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place testpoint on H_IERR# with a GND 0.1" away
Layout Note: "CPU_GTLREF0" 0.5" max length.
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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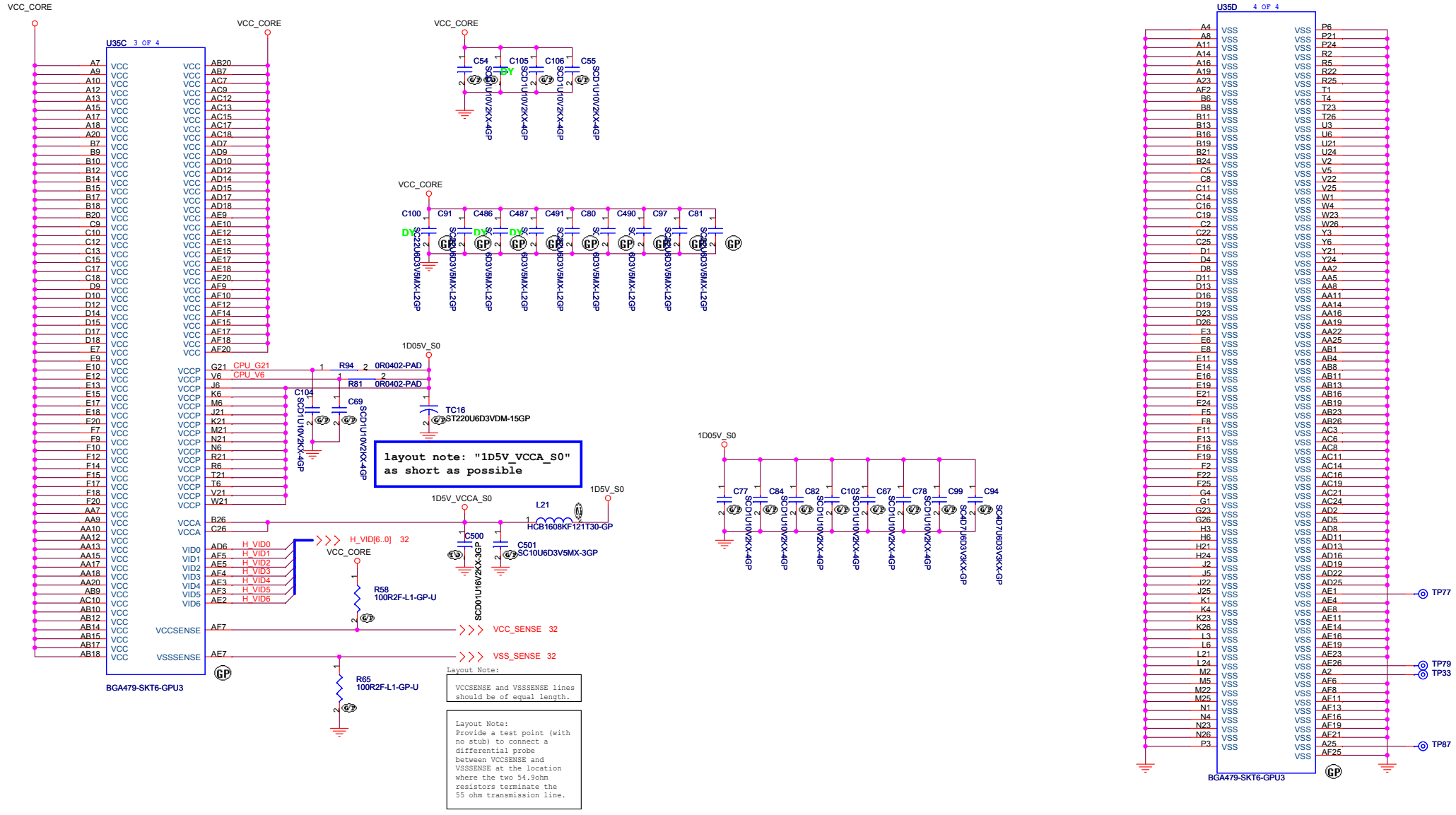
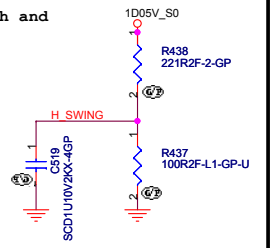
CPU (1 of 2)
D45/D46
PD
Friday, March 14, 2008
Sheet 4 of 47



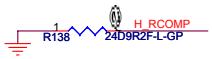
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CPU (2 of 2)		
Size	Document Number		Rev
	D45/D46		PD
Date: Friday, March 14, 2008	Sheet 5	of	47

H_SWING routing Trace width and Spacing use 10 / 20 mil

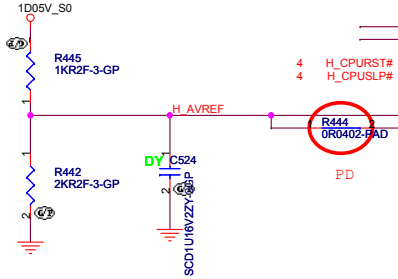
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)

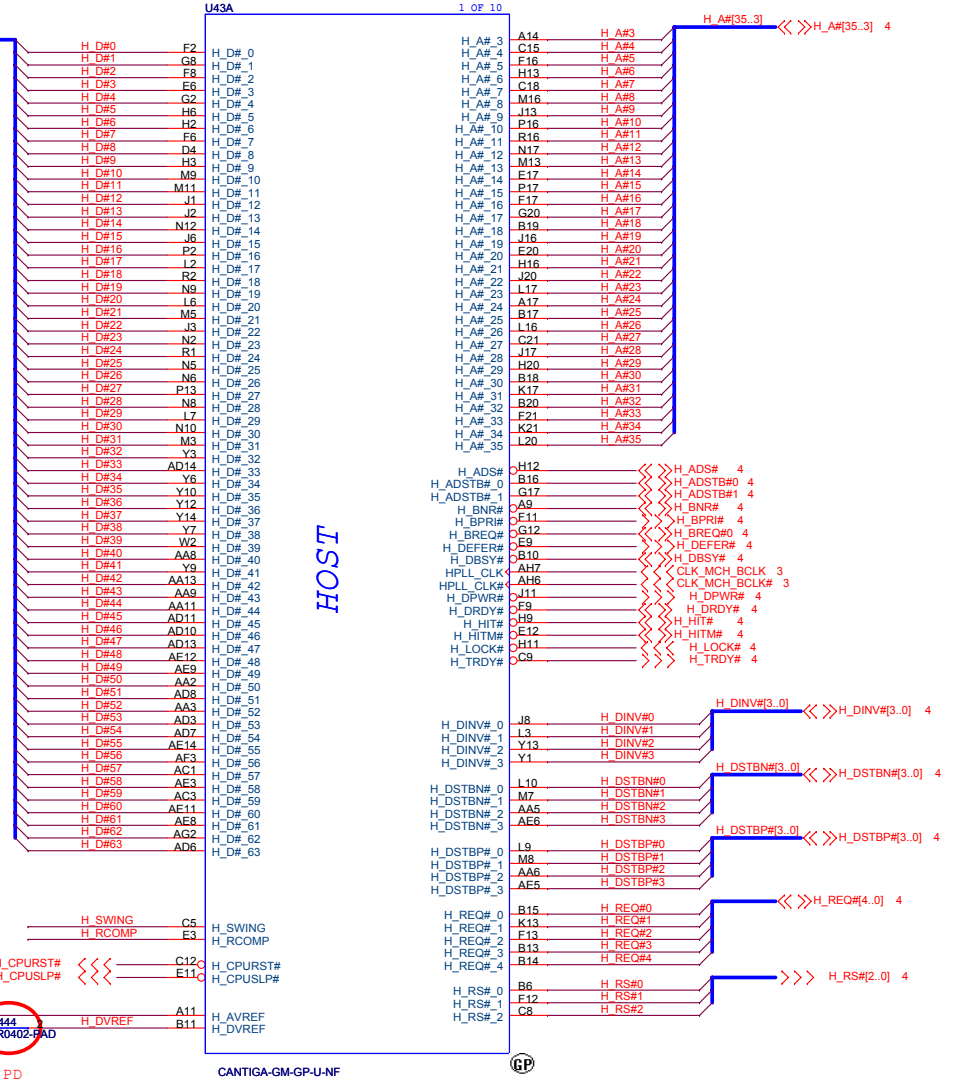


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")





D45 SB use 71.CNTIG.H0U

D46 SB use 71.CNTIG.G0U

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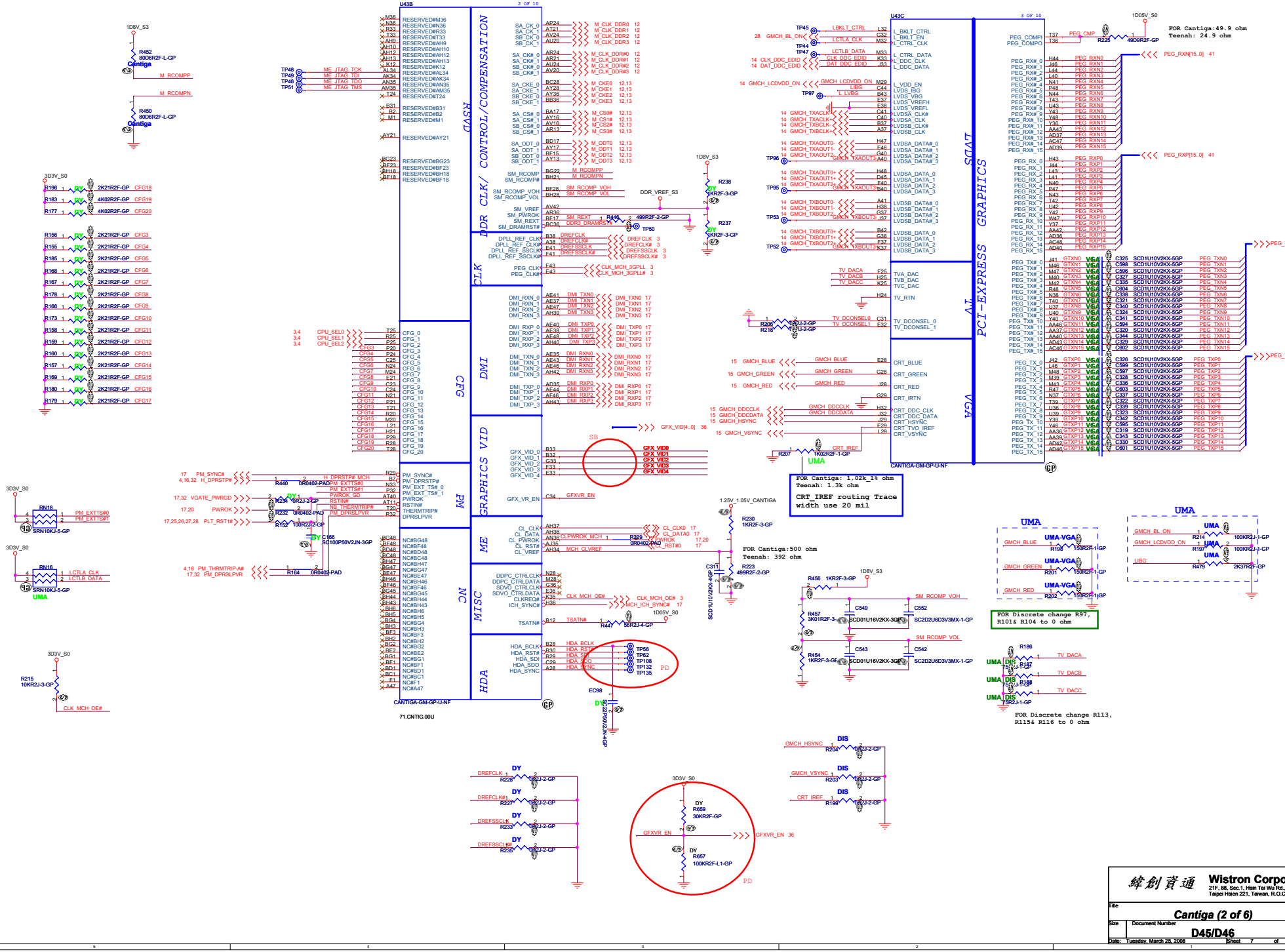
Title: Cantiga (1 of 6)		
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 6 of 47	


U43B
2 OF 10
HOST
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
DDR CLK/ CONTROL/COMPENSATION
U43C
3 OF 10
PCI-EXPRESS GRAPHICS
TVDAC
VGA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
FOR Cantiga:49.9 ohm
Teenah: 24.9 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Discrete change R97, R101& R104 to 0 ohm
FOR Discrete change R113, R115& R116 to 0 ohm
UMA
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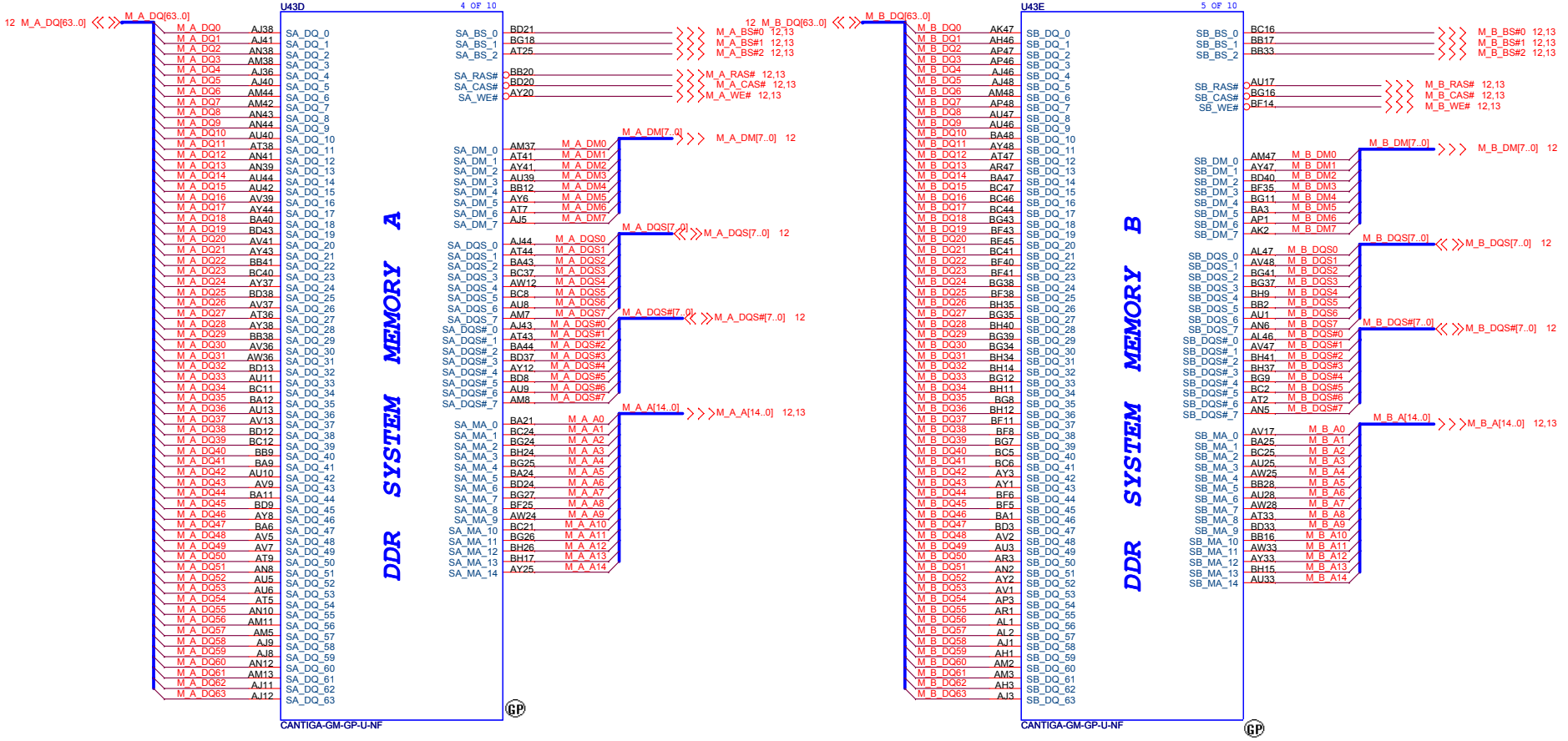
Cantiga (2 of 6)
D45/D46
Tuesday, March 25, 2008



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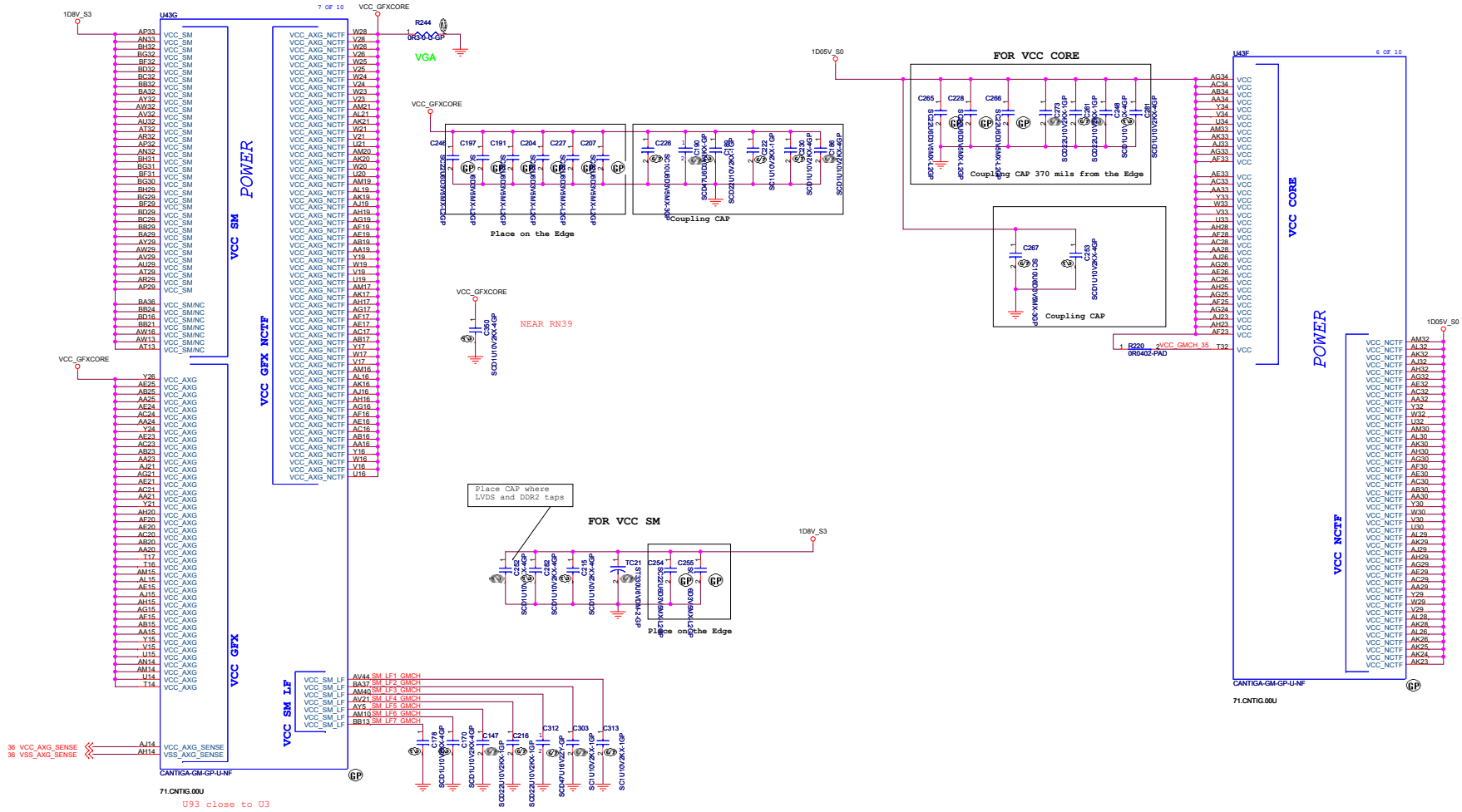
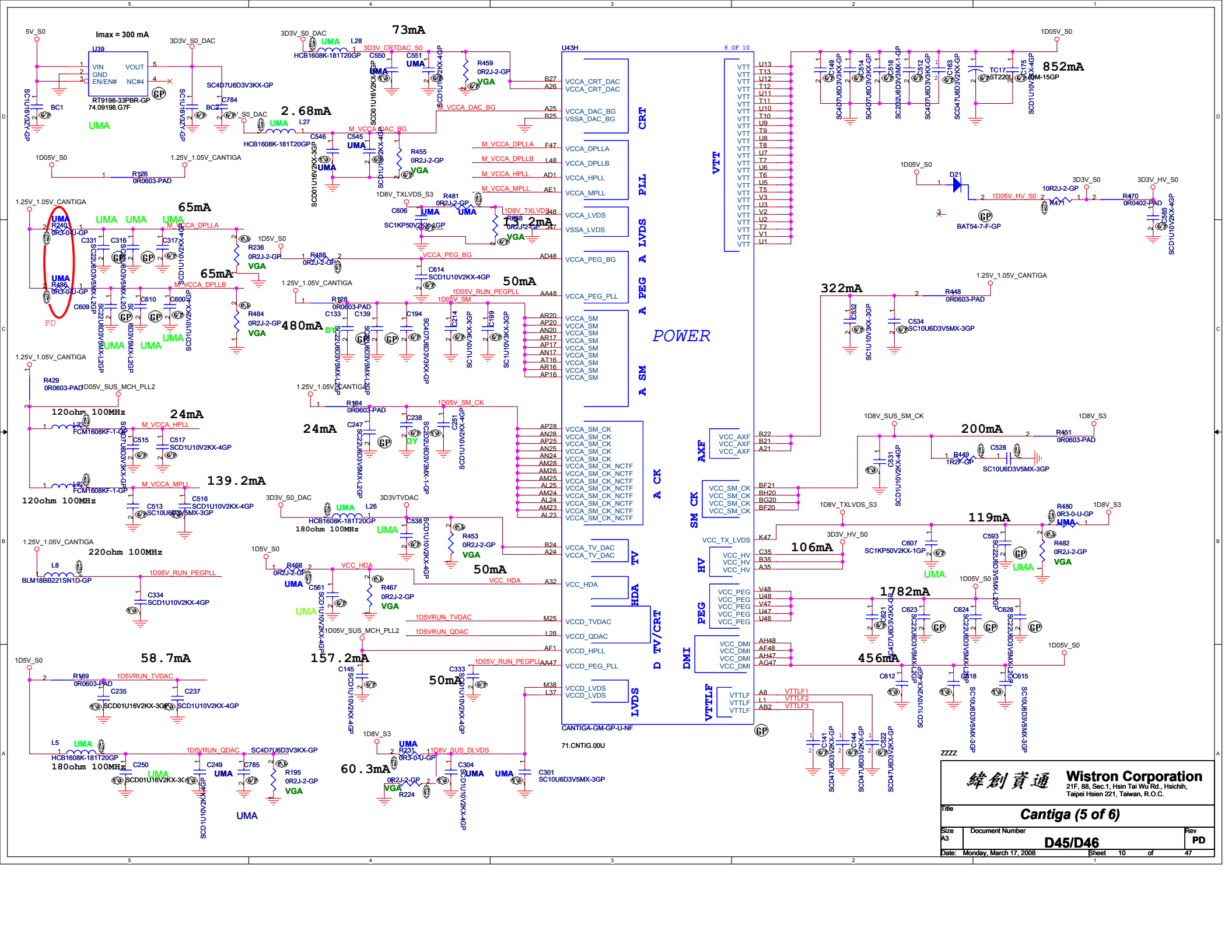
Title: **Cantiga (3 of 6)**

Size	Document Number	Rev
	D45/D46	PD

Date: Friday, March 14, 2008 Sheet 8 of 47



Wistron Corporation	Title: Cantiga (4 of 6)	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: Document Number: D45/D46	Rev: PD
	Date: Monday, March 24, 2008	Sheet 9 of 47


POWER
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
73mA
2.68mA
65mA
65mA
480mA
50mA
24mA
139.2mA
58.7mA
157.2mA
50mA
60.3mA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
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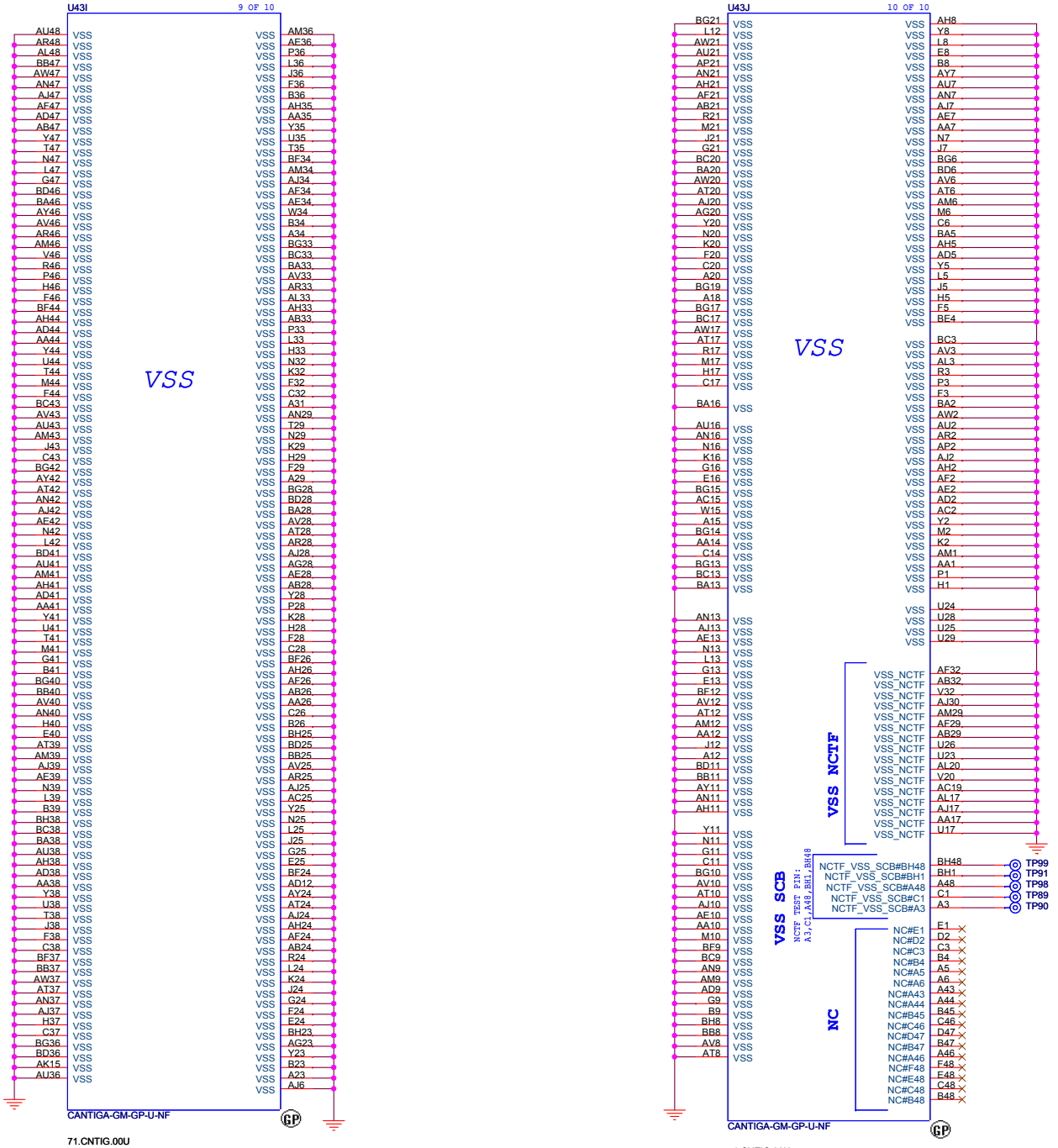
Cantiga (5 of 6)
D45/D46
PD
Monday, March 17, 2008
Sheet 10 of 47



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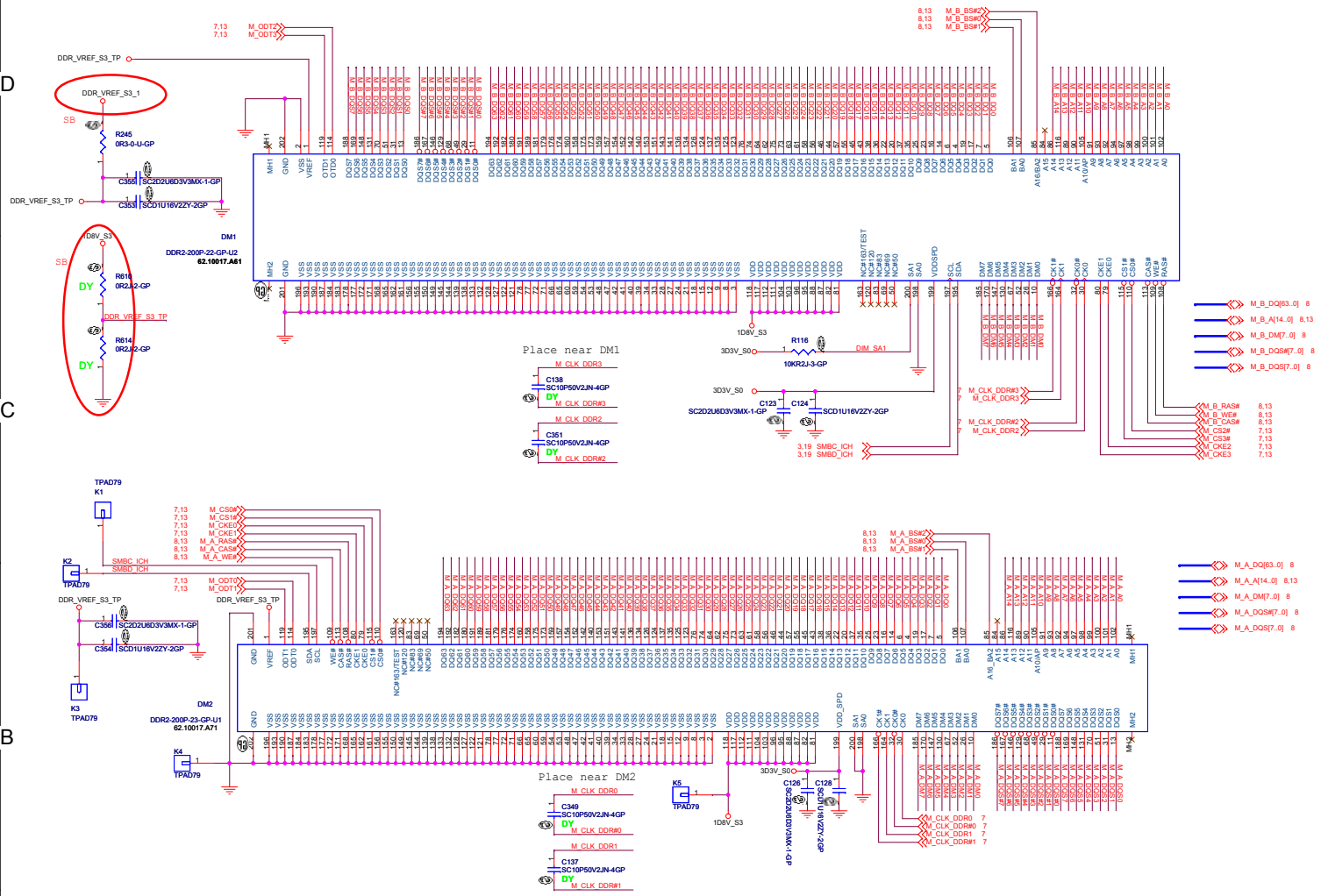
Title	***Cantiga (6 of 6)***	
Size	Document Number: **D45/D46**	Rev: **PD**
Date: Friday, March 14, 2008	Sheet 11 of 47	

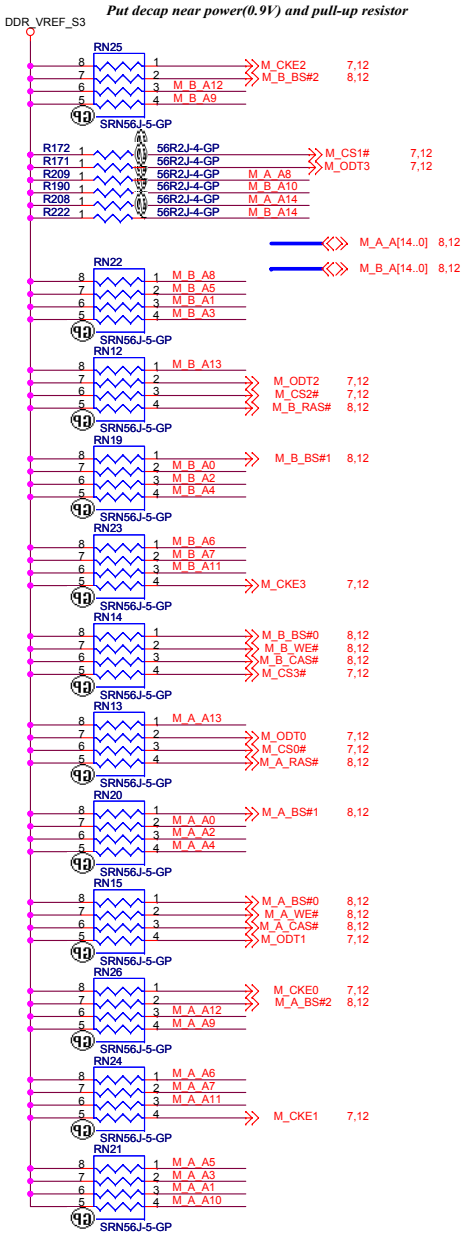
DDR SOCKET



D45 46 use 62.10017.G31

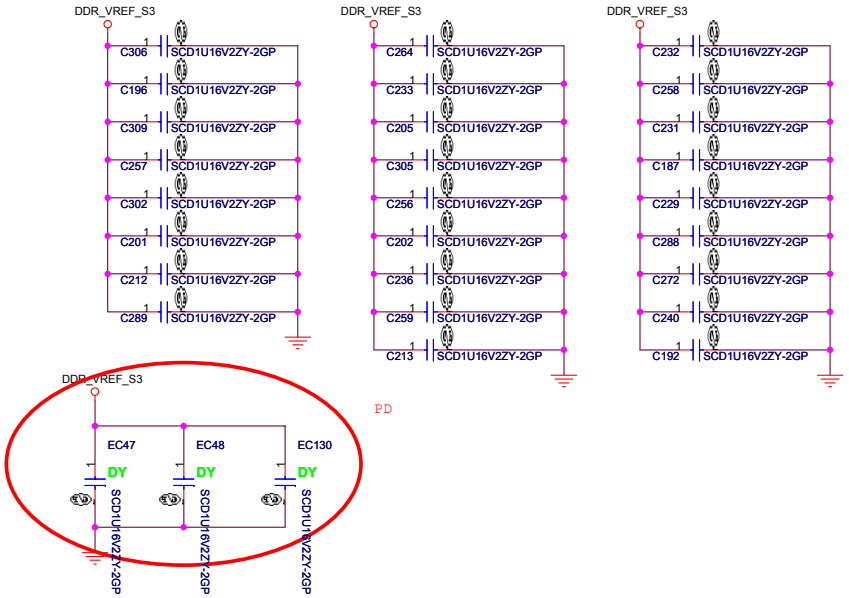
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR2 Socket	
Size	Document Number: D45/D46 Rev: PD
Date: Friday, March 14, 2008	Sheet 12 of 47

PARALLEL TERMINATION

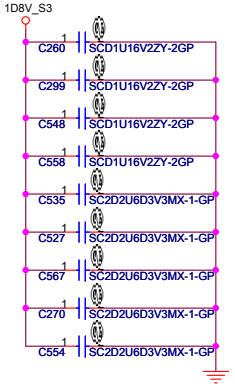


Decoupling Capacitor

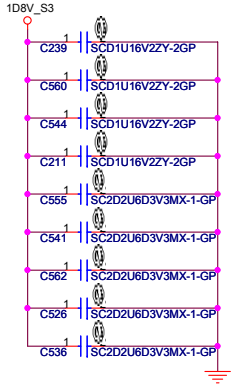
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



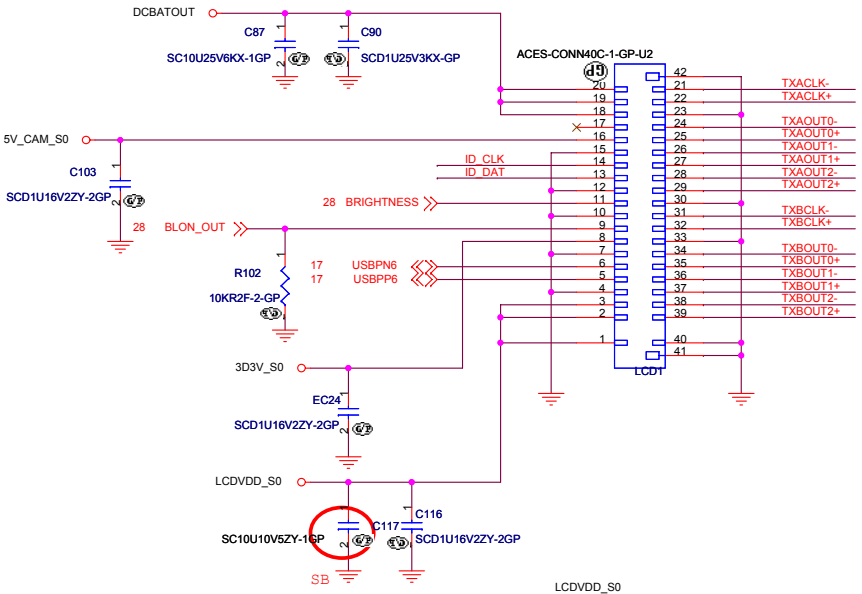
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

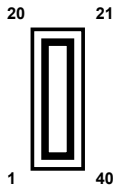
Size	Document Number	Rev
	D45/D46	PD

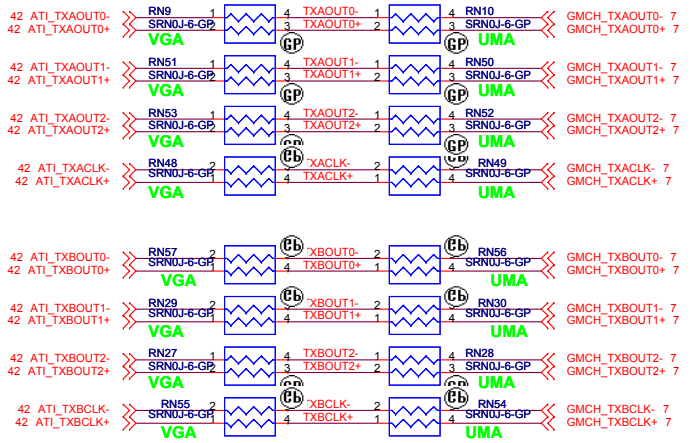
Date: Wednesday, March 19, 2008 Sheet 13 of 47

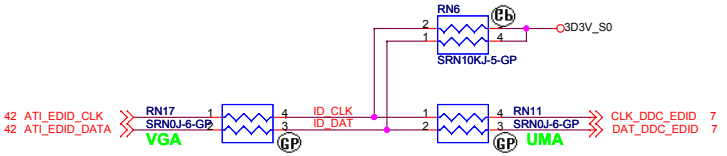
LCD CONNECTOR

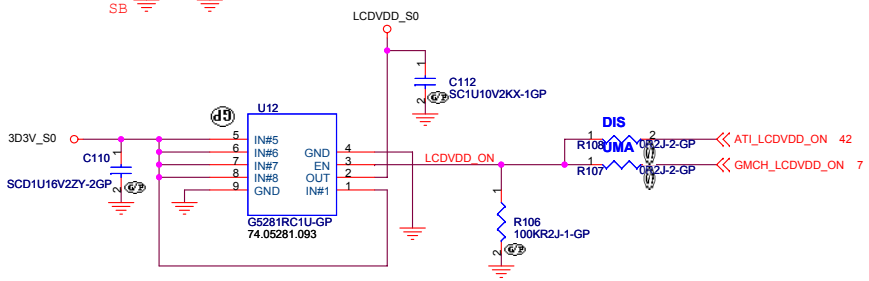


TOP VIEW

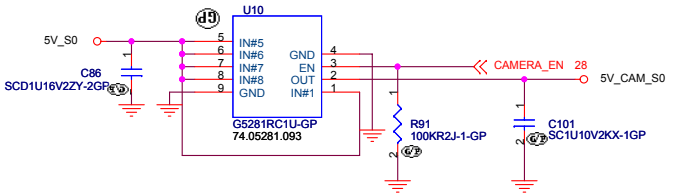


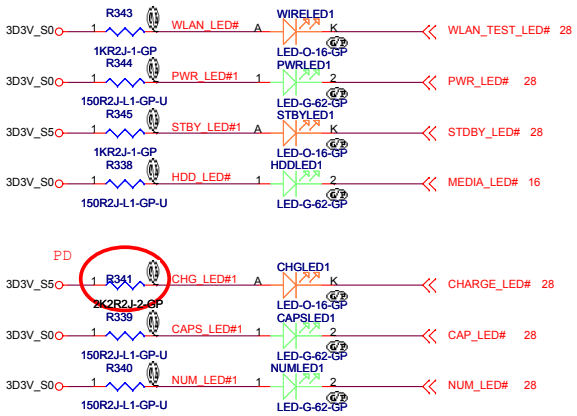




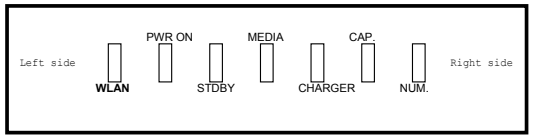


WEBCAM POWER





LED Location and Sequence (The edge of PCB,Top view)



zzzz

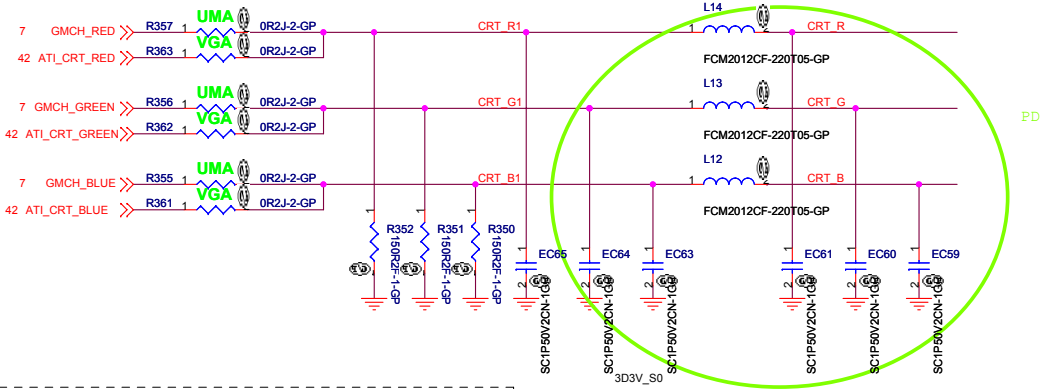
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LCD CONN / LED / WEBCAM***
Size A3 / Document Number	**D45/D46** / Rev **PD**
Date: Friday, March 14, 2008	Sheet 14 of 47

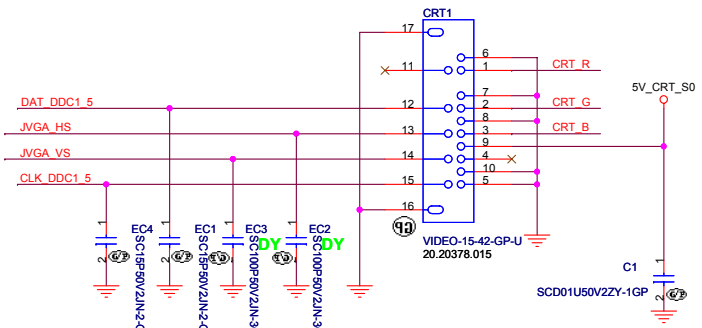
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

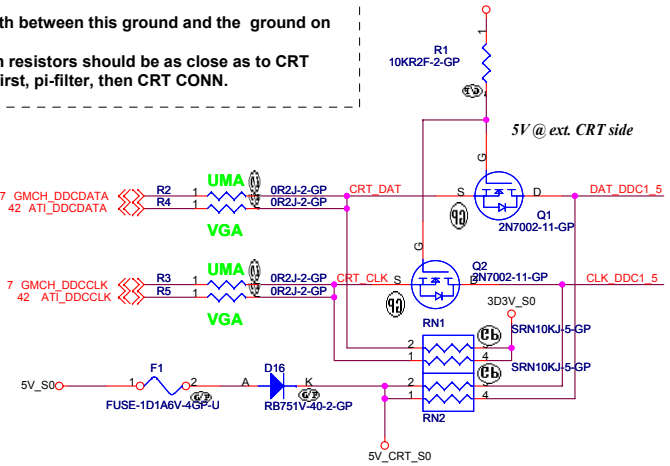
Ferrite bead impedance: 10 ohm@100MHz

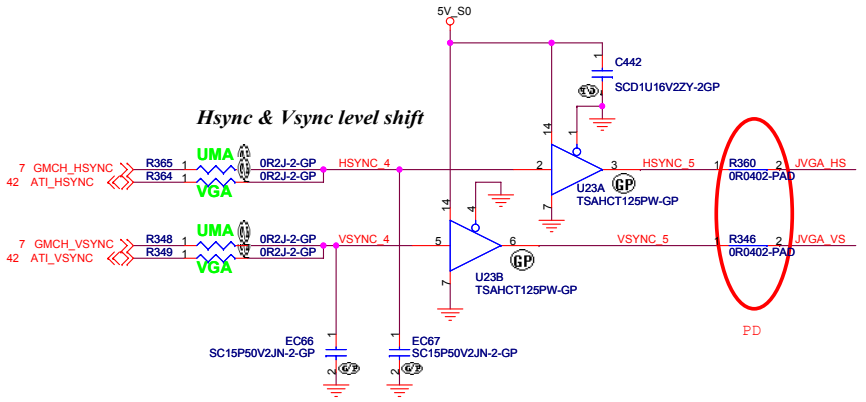
PD use 22 ohm 68.00215.211

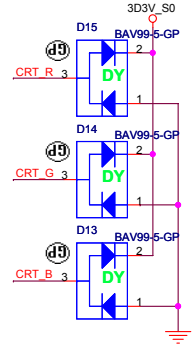




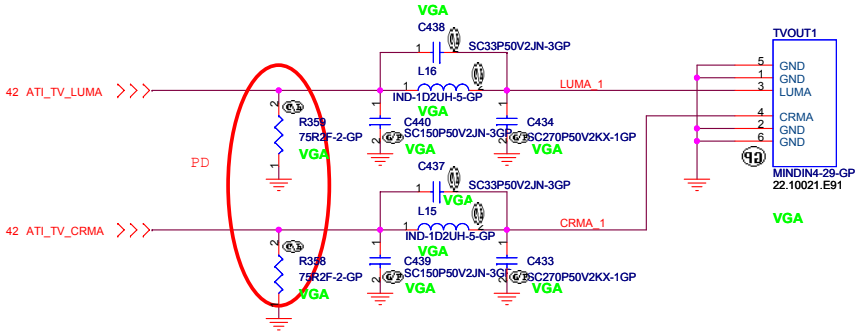
Layout Note:
*** Must be a ground return path between this ground and the ground on the VGA connector.**
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

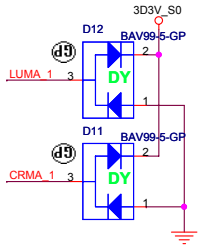






TV CONN



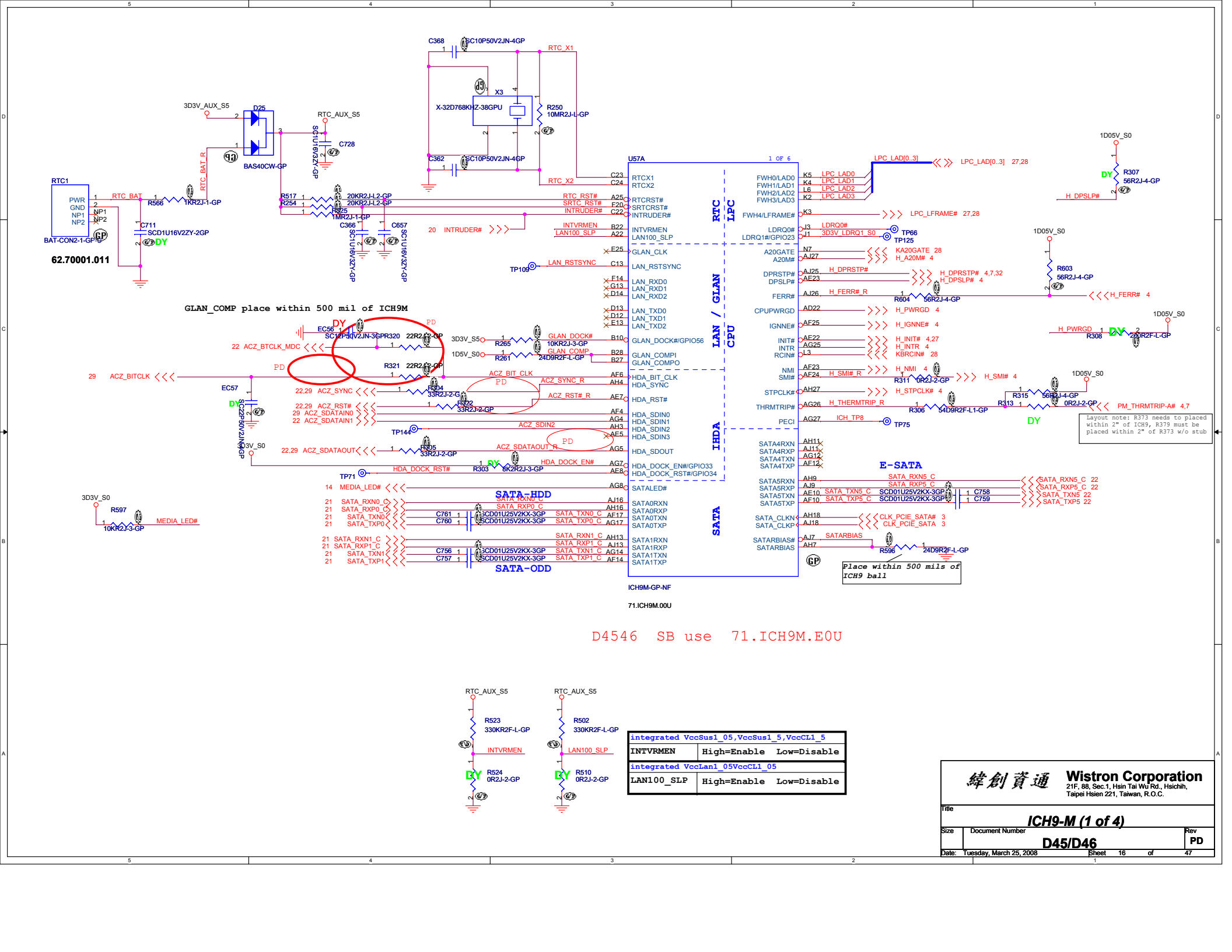


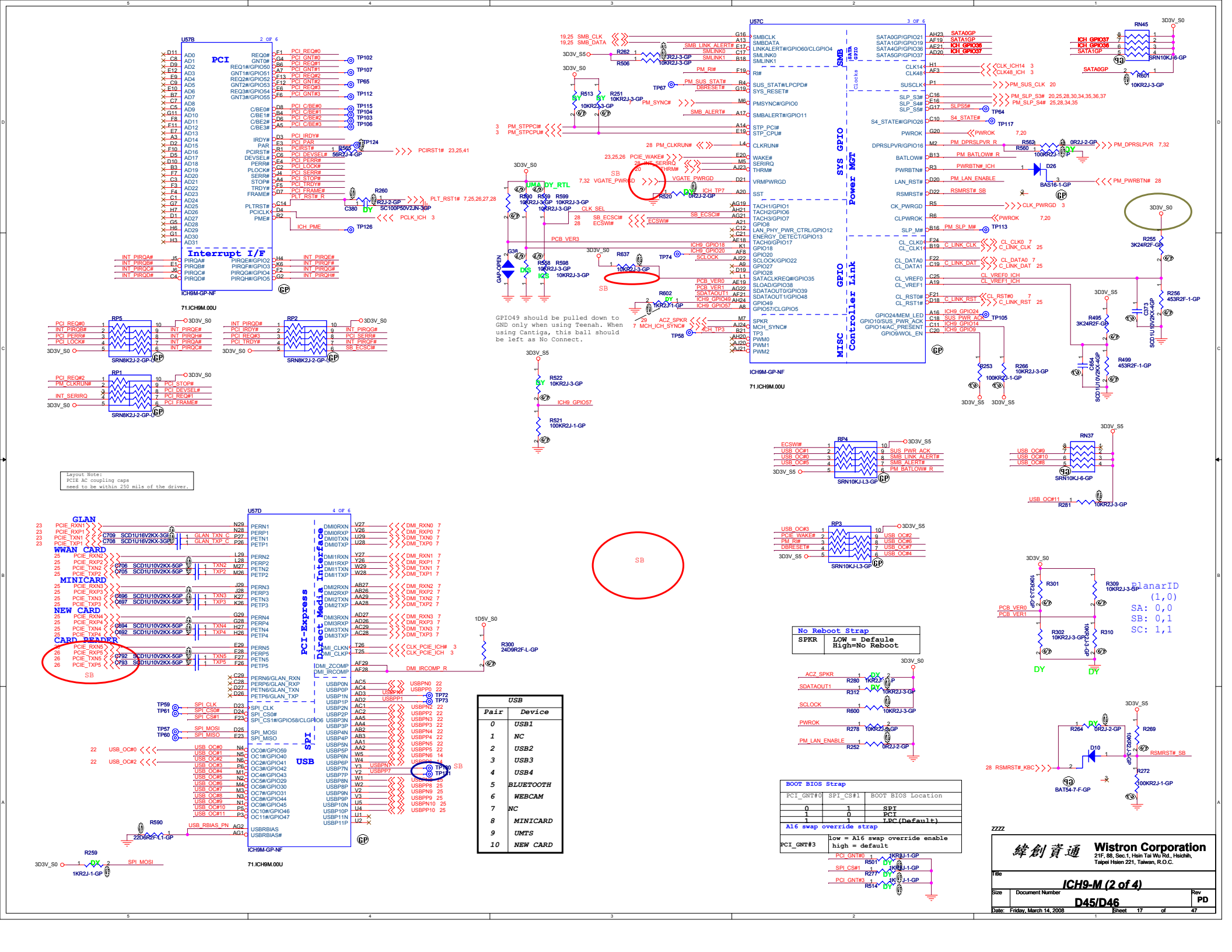
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

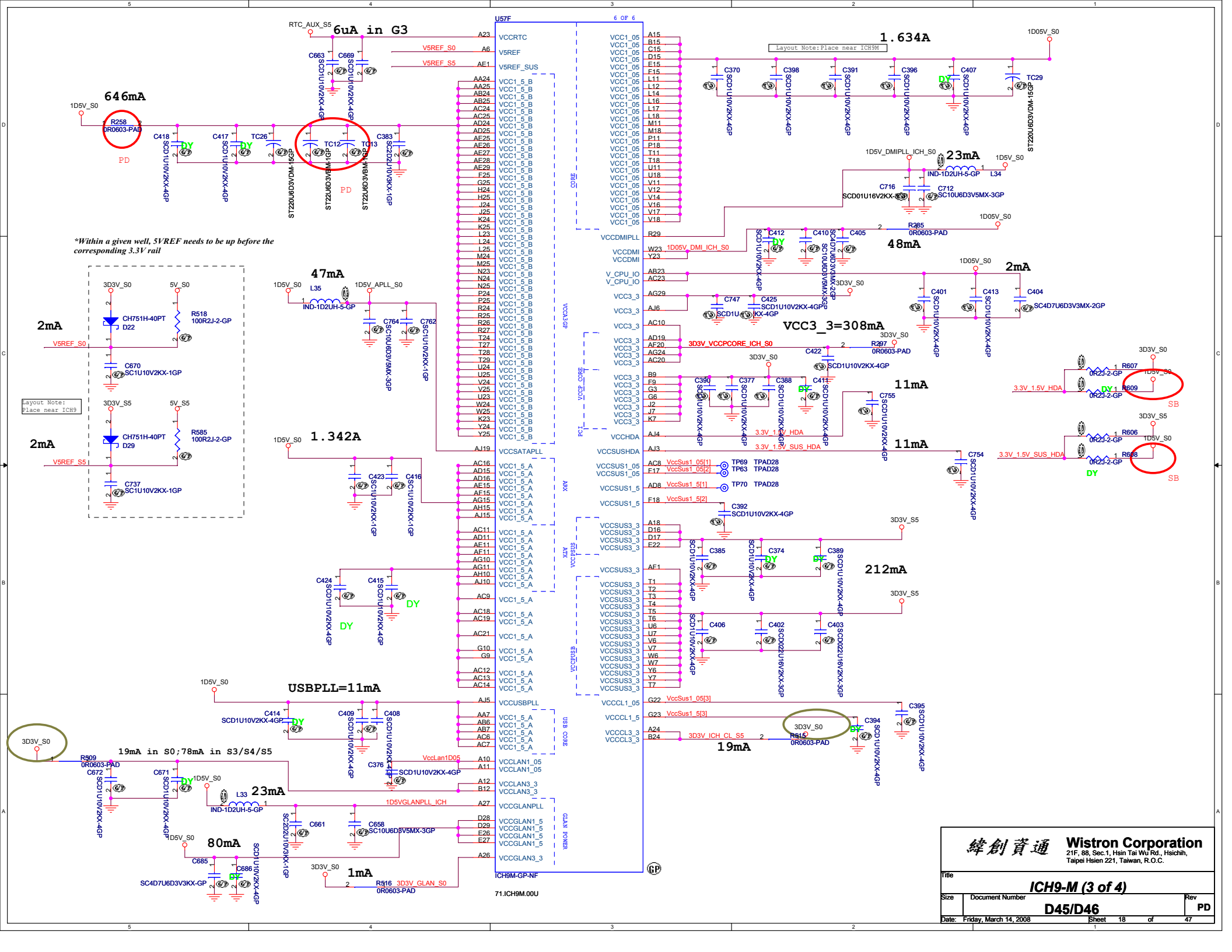
Title: **CRT/TV Connector**

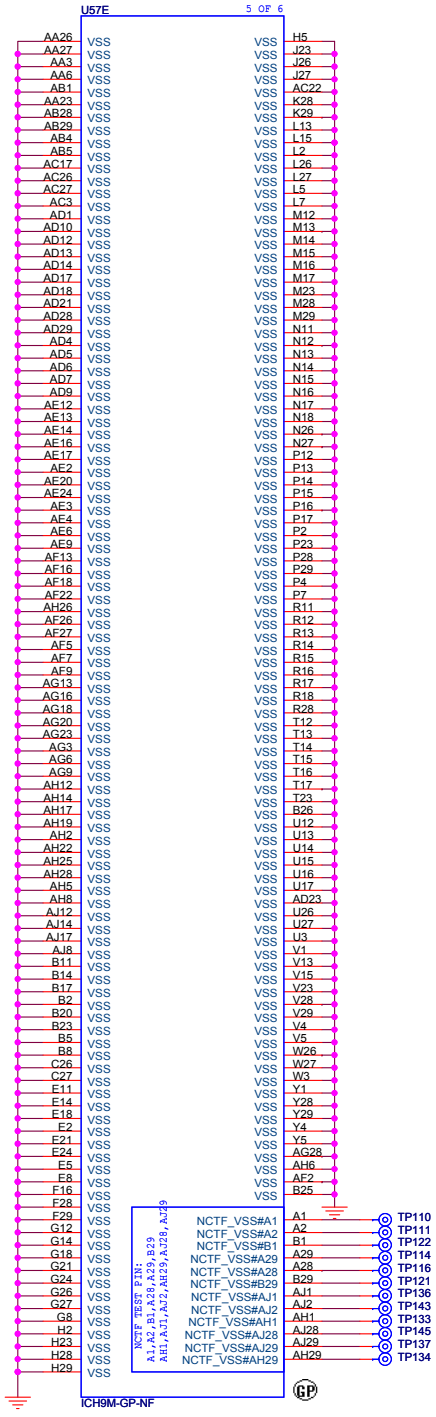
Size | Document Number: **D45/D46** | Rev: **PD**

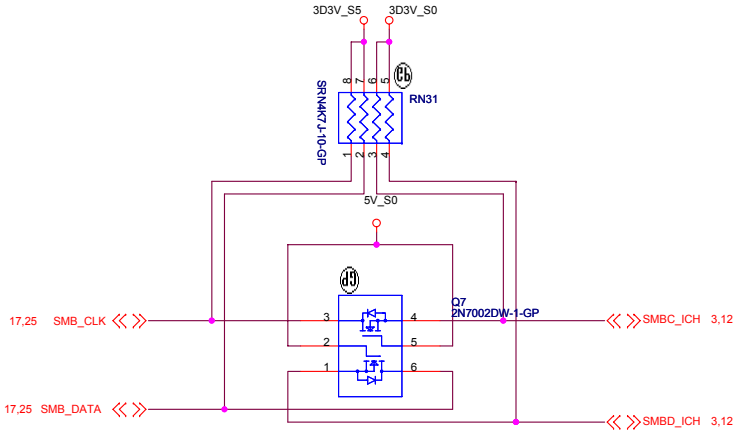
Date: Tuesday, March 18, 2008 | Sheet 15 of 47


GLAN_COMP place within 500 mil of ICH9M
SATA-HDD
SATA-ODD
E-SATA
U57A
ICH9M-GP-NF
71.ICH9M.00U
62.70001.011
D4546 SB use 71.ICH9M.E0U
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
Place within 500 mils of ICH9 ball
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
D45/D46
PD
Date: Tuesday, March 25, 2008
Sheet 16 of 47


U57B
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
U57C
SMB
GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
U57D
GLAN
WWAN CARD
MINICARD
NEW CARD
CARD READER
PCI-Express
Direct Media Interface
SPI
USB
SB
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
USB
Pair
Device
0
USB1
1
NC
2
USB2
3
USB3
4
USB4
5
BLUETOOTH
6
WEBCAM
7
NC
8
MINICARD
9
UMTS
10
NEW CARD
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC (Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,1
ZZZZ
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
D45/D46
Rev
PD
Date: Friday, March 14, 2008
Sheet 17 of 47


6uA in G3
646mA
1.634A
23mA
48mA
2mA
47mA
1.342A
VCC3_3=308mA
11mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
U57F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
D45/D46
PD
Friday, March 14, 2008
Sheet 18 of 47



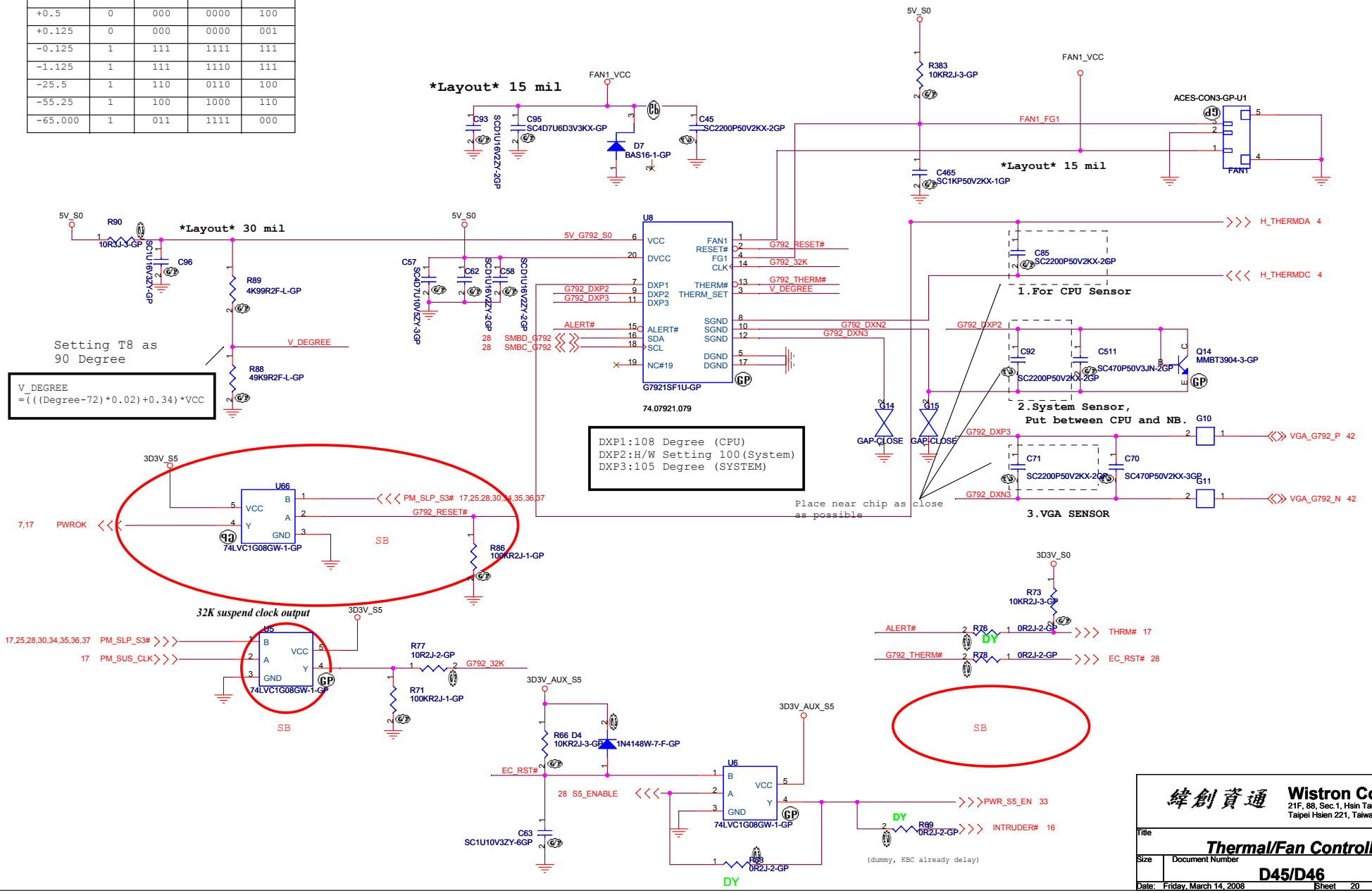


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *ICH9-M (4 of 4)*		
Size	Document Number: D45/D46	Rev: PD
Date: Friday, March 14, 2008	Sheet 19 of 47	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



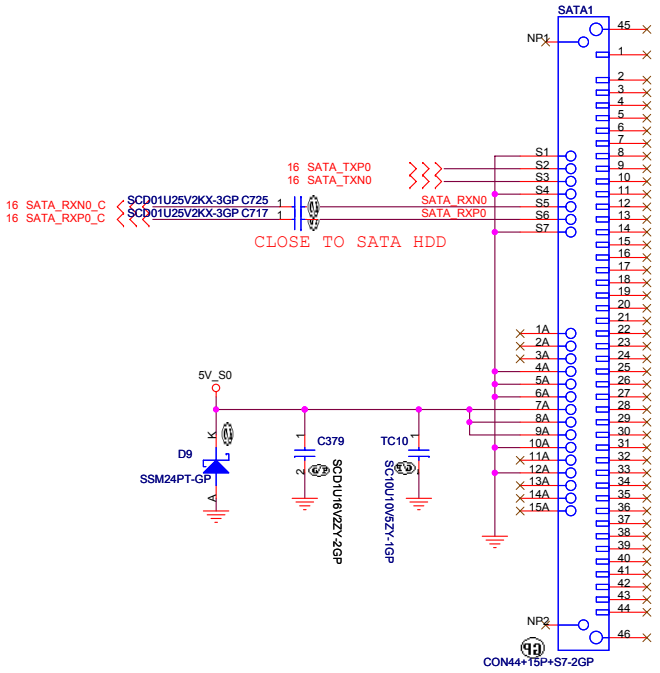
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controllor**

Size | Document Number: **D45/D46** | Rev: PD

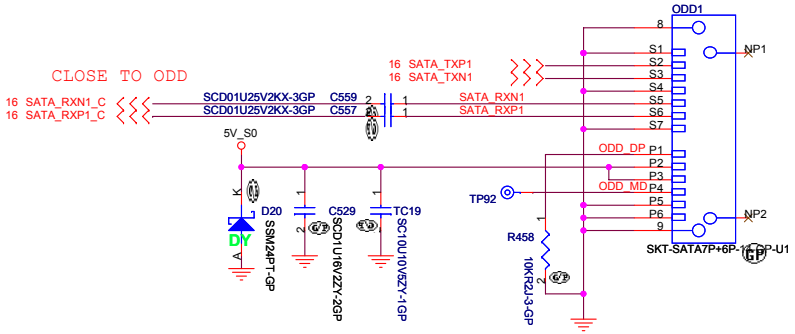
Date: Friday, March 14, 2008 | Sheet 20 of 47

SATA HD Connector

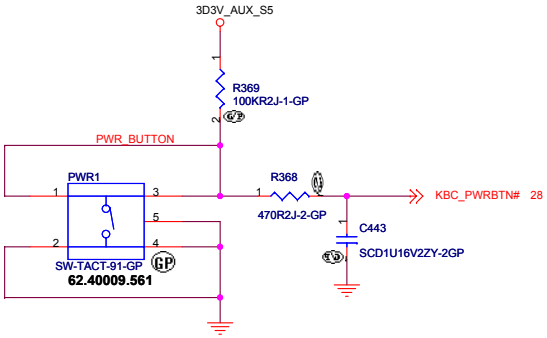


20.F0885.001

ODD Connector

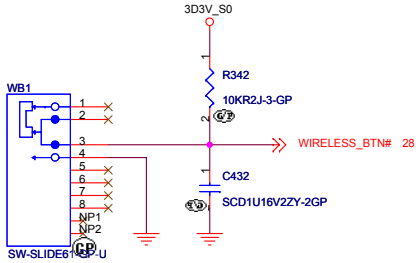


LAUNCH BUTTON



62.40009.561

WIRELESS BUTTON

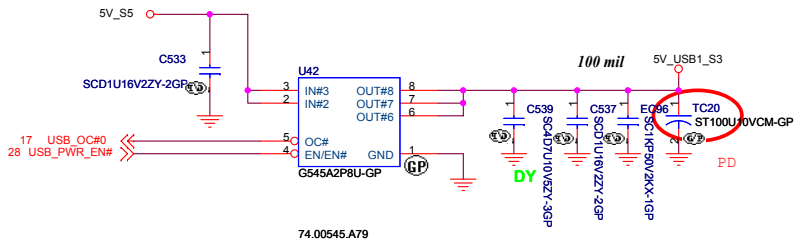


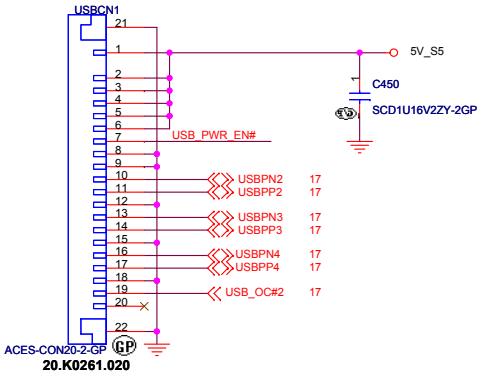
62.40018.351

ZZZZ

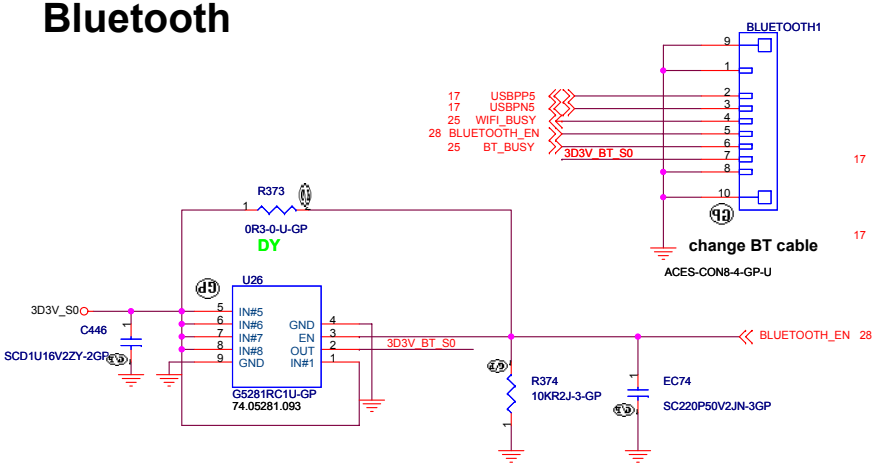
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD / CDROM / LAUNCH	
Size	Document Number D45/D46	Rev PD
Date: Friday, March 14, 2008	Sheet 21 of 47	

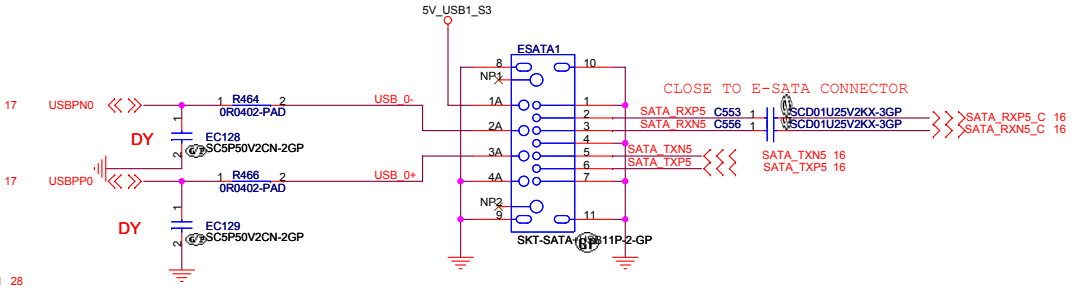
USB BOARD CONN





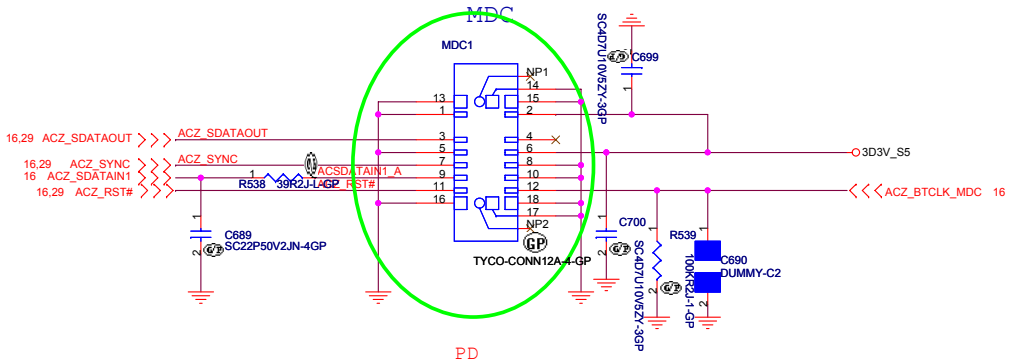
Bluetooth





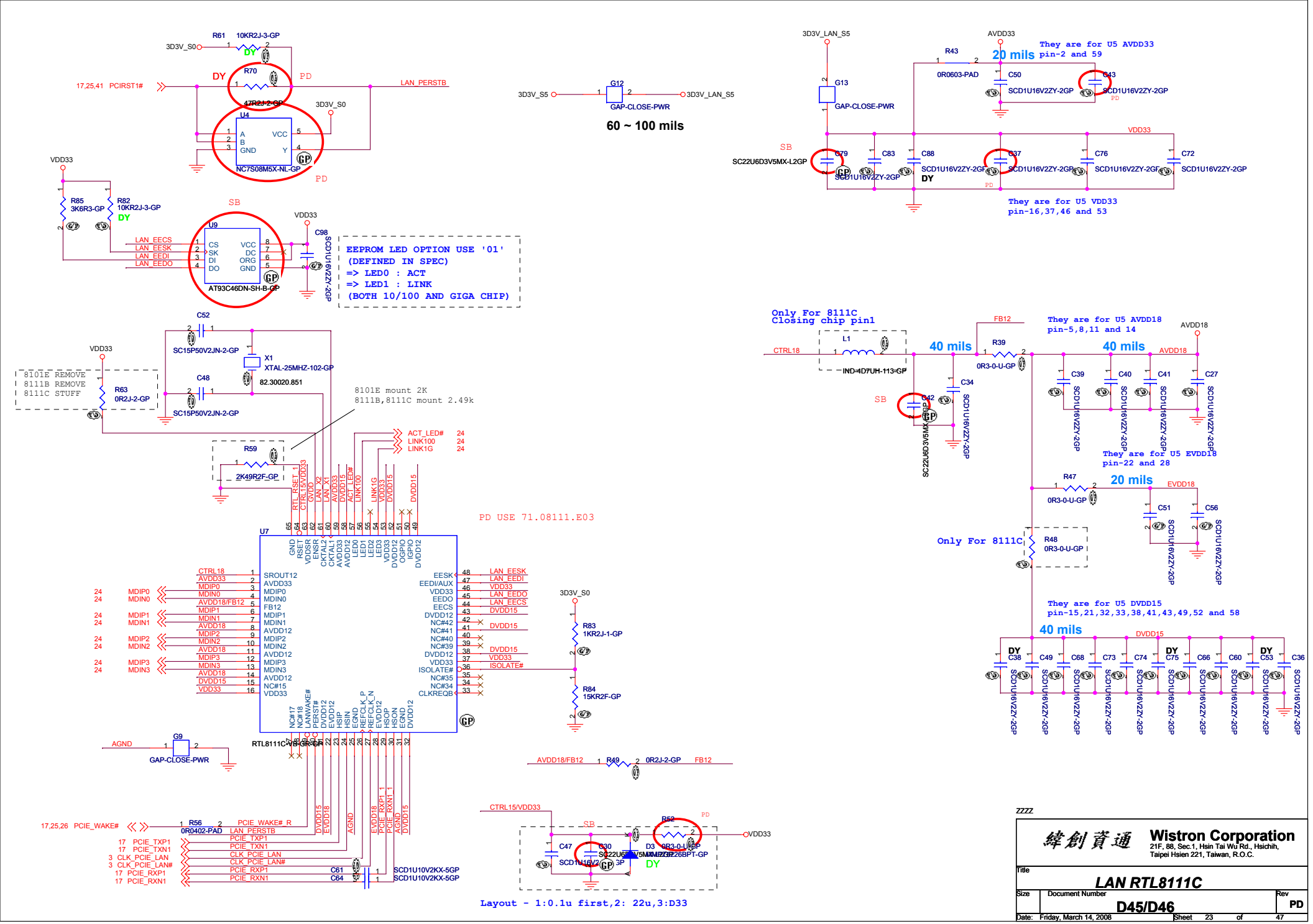
PD USE 22.10218.Z71

eSATA/USB



ZZZZ

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC / BLUETOOTH***	
Size	Document Number **D45/D46**	Rev **PD**
Date: Friday, March 14, 2008	Sheet 22 of 47	



ZZZZ

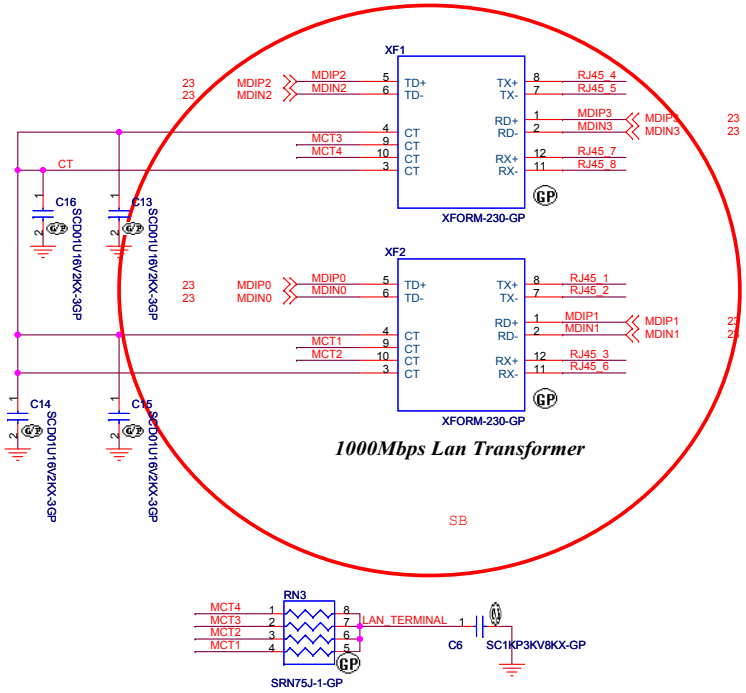
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

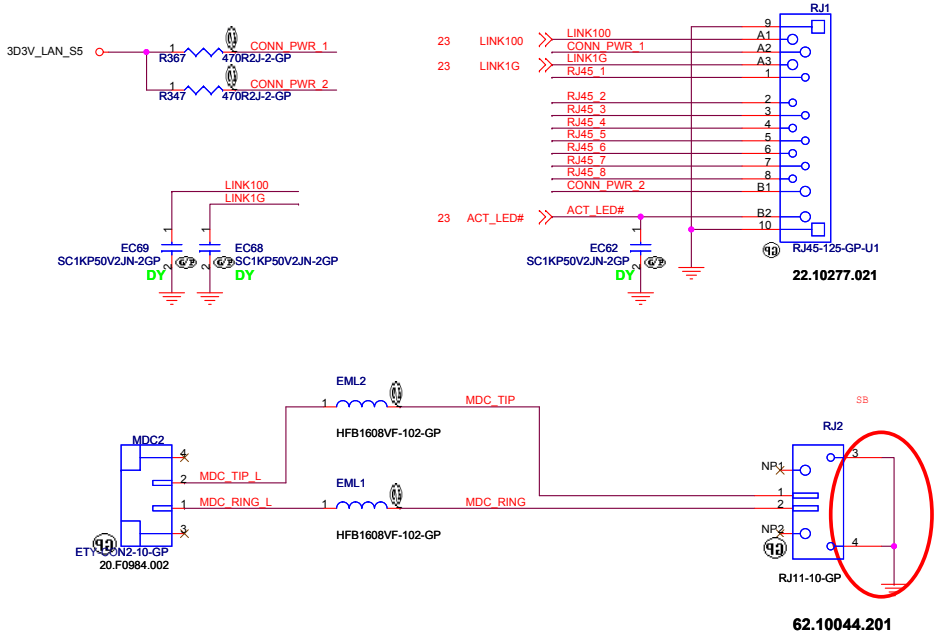
Title: **LAN RTL8111C**

Size | Document Number: **D45/D46** | Rev: PD

Date: Friday, March 14, 2008 | Sheet 23 of 47

Lan Conn





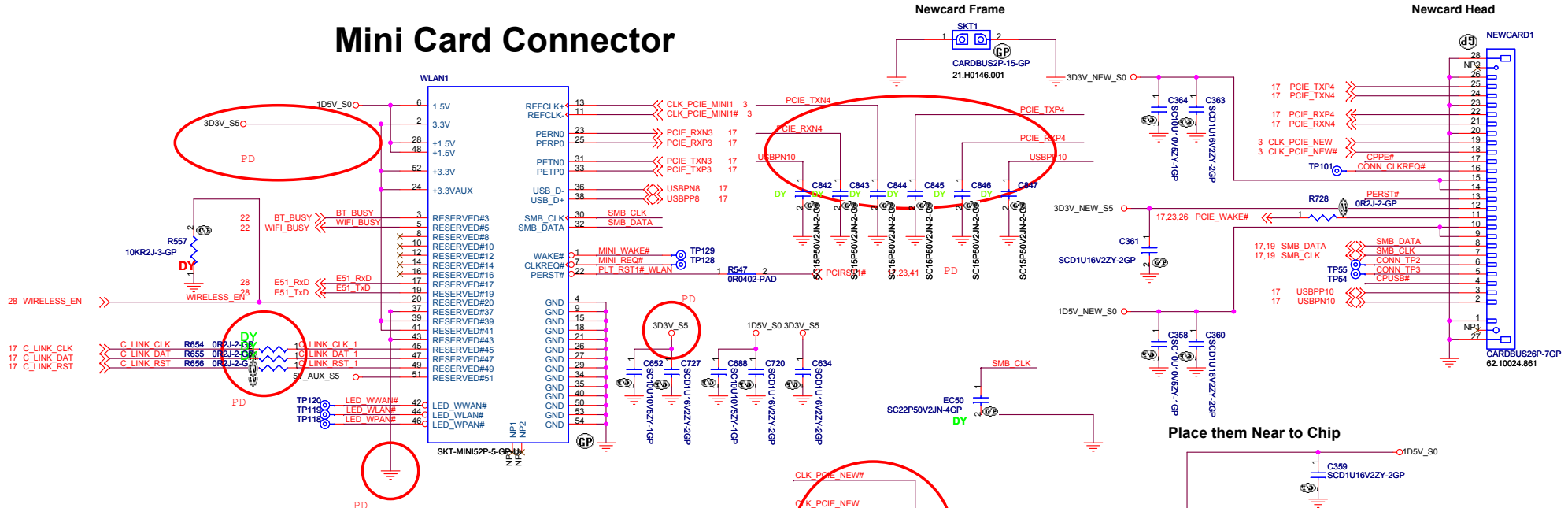
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

ZZZZ

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***LAN Connector***	
Size	Document Number **D45/D46**	Rev **PD**
Date: Friday, March 14, 2008	Sheet 24 of 47	

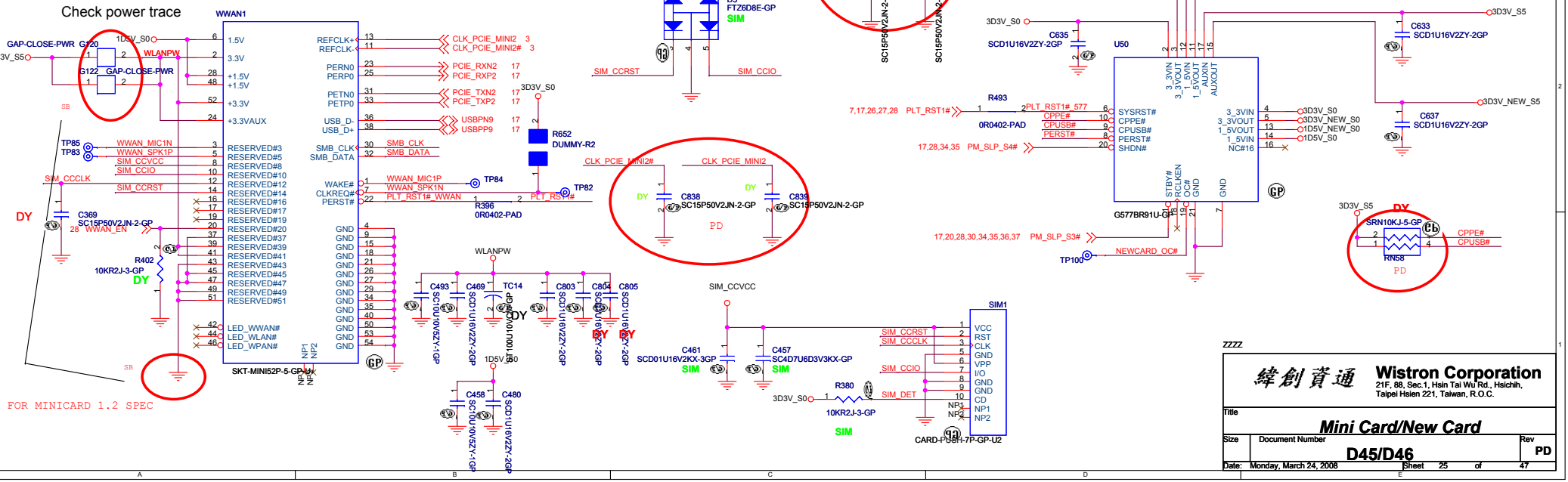
Mini Card Connector



WWAN Connector

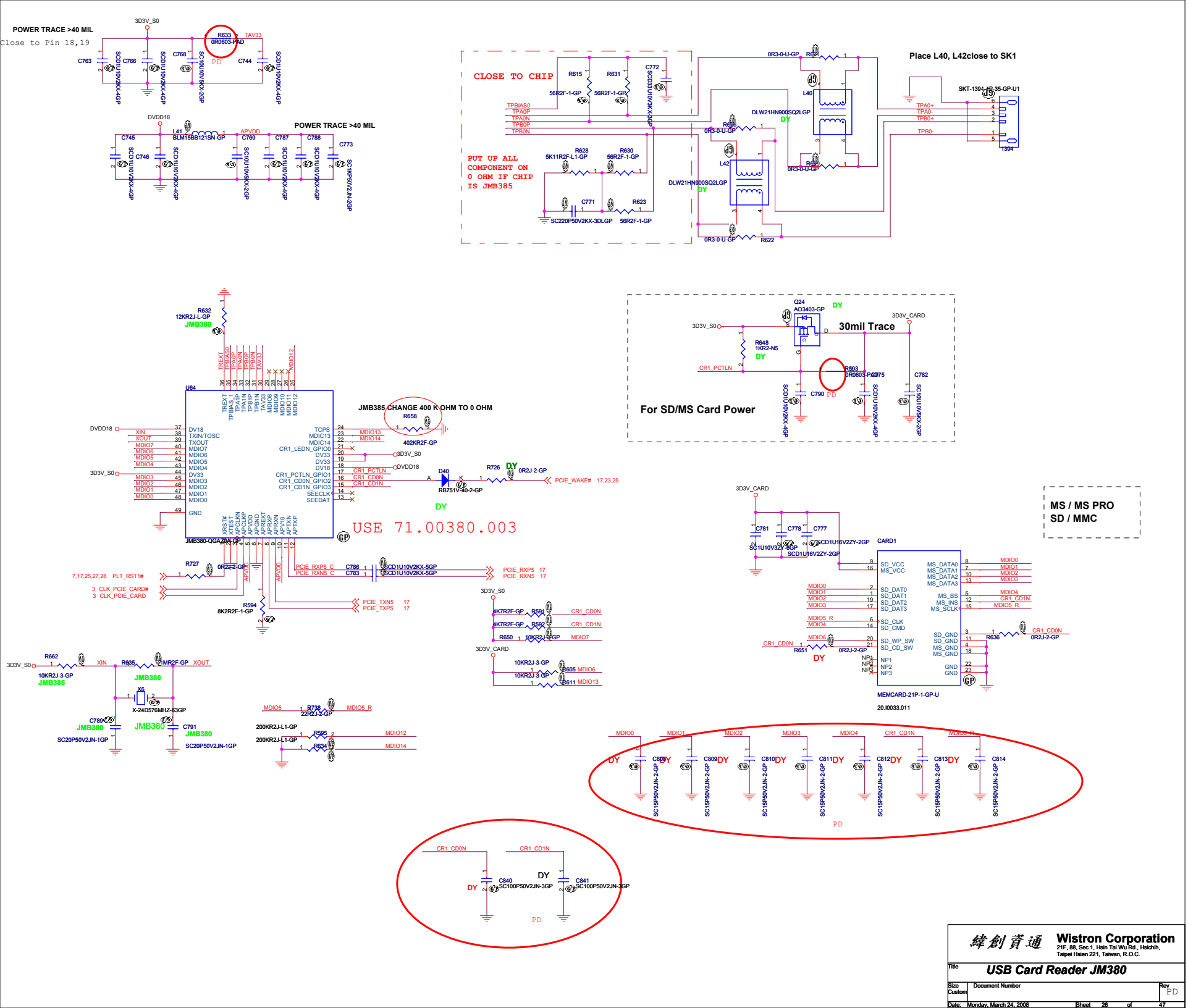
(ROBISON RESERVE)

Check power trace



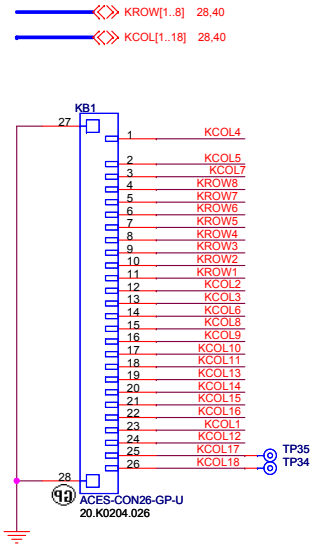
ZZZZ

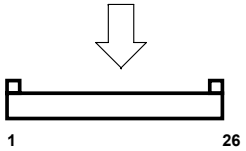
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Mini Card/New Card***	
Size	Document Number **D45/D46**	Rev **PD**
Date: Monday, March 24, 2008	Sheet 25 of 47	



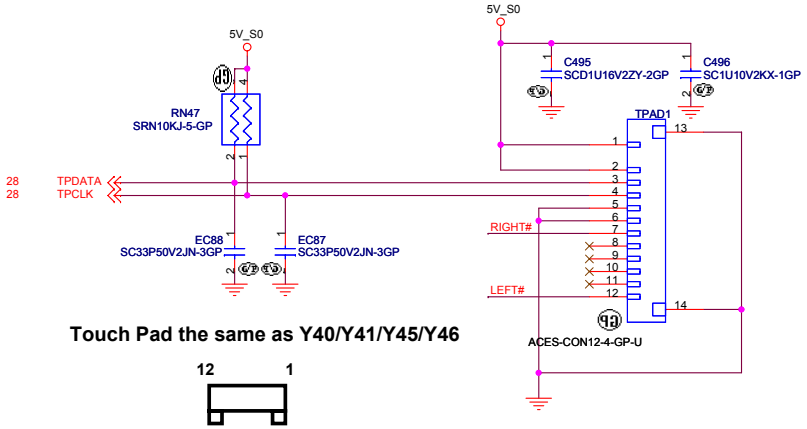
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB Card Reader JM380			
Size: Custom	Document Number		Rev: PD
Date: Monday, March 24, 2008	Sheet 26 of 47		

Internal KeyBoard Connector

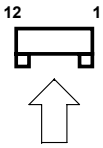




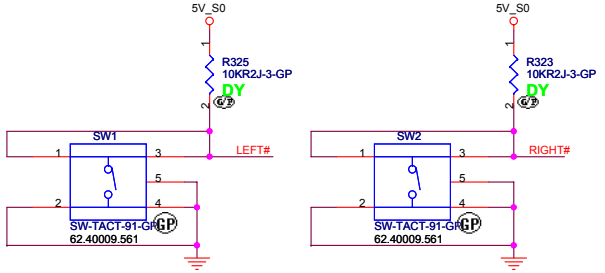
TouchPad Connector



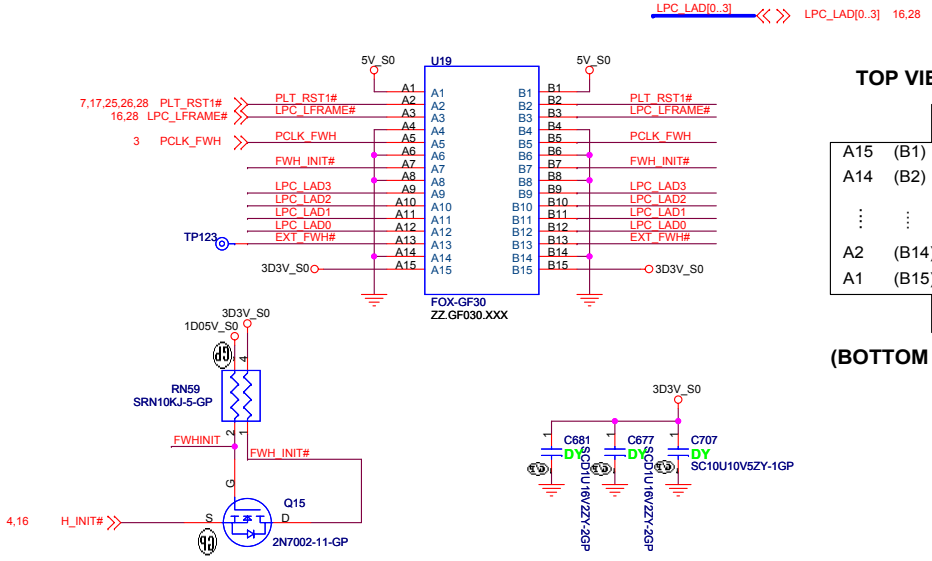
Touch Pad the same as Y40/Y41/Y45/Y46



15" TOUCHPAD BUTTON SWITCH



GOLDEN FINGER FOR DEBUG BOARD

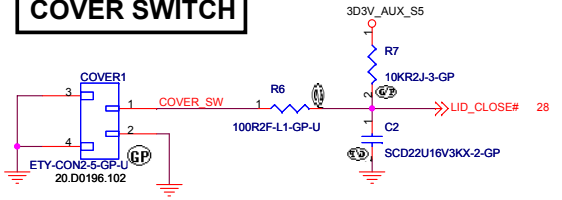


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

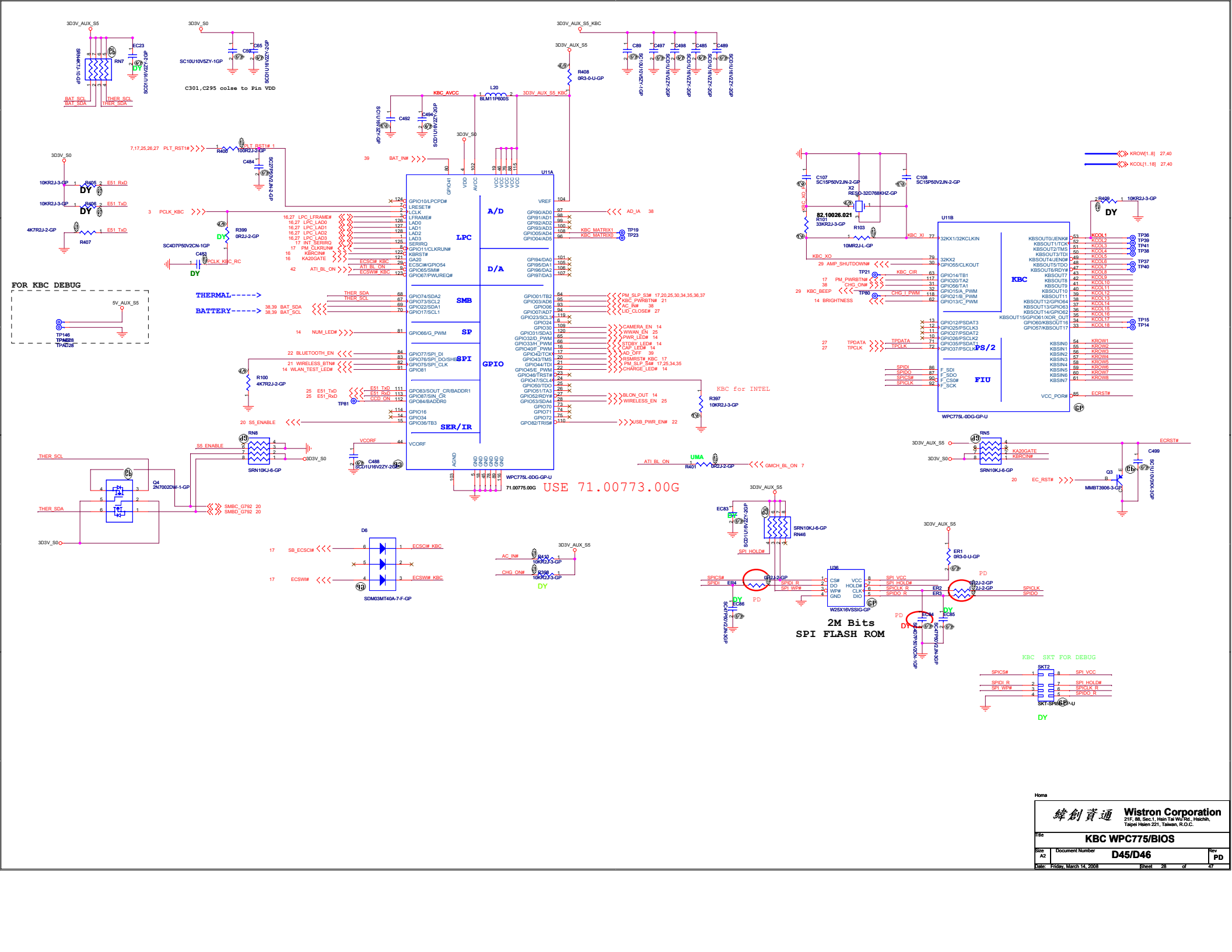
(BOTTOM VIEW)

COVER SWITCH



zzzz

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***KeyBoard/TPAD/Debug***	
Size: Custom	Document Number: **D45/D46**	Rev: PD
Date: Tuesday, March 25, 2008	Sheet 27 of 47	



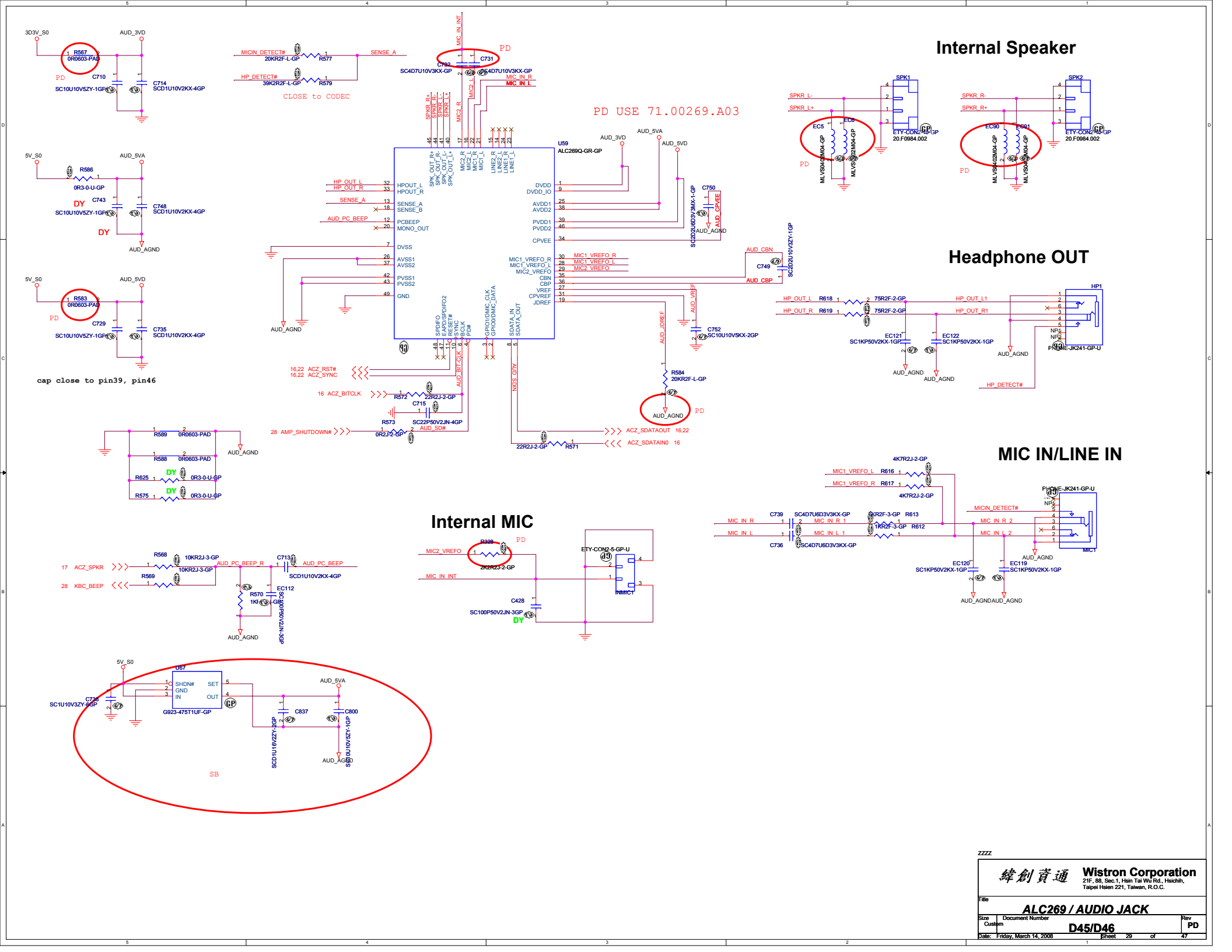
Homa

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

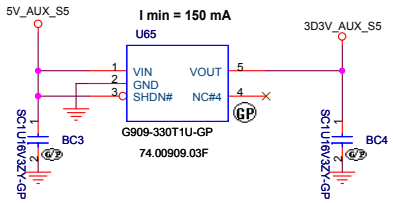
Title: KBC WPC775/BIOS

Size	Document Number	Rev
A2	D45/D46	PD

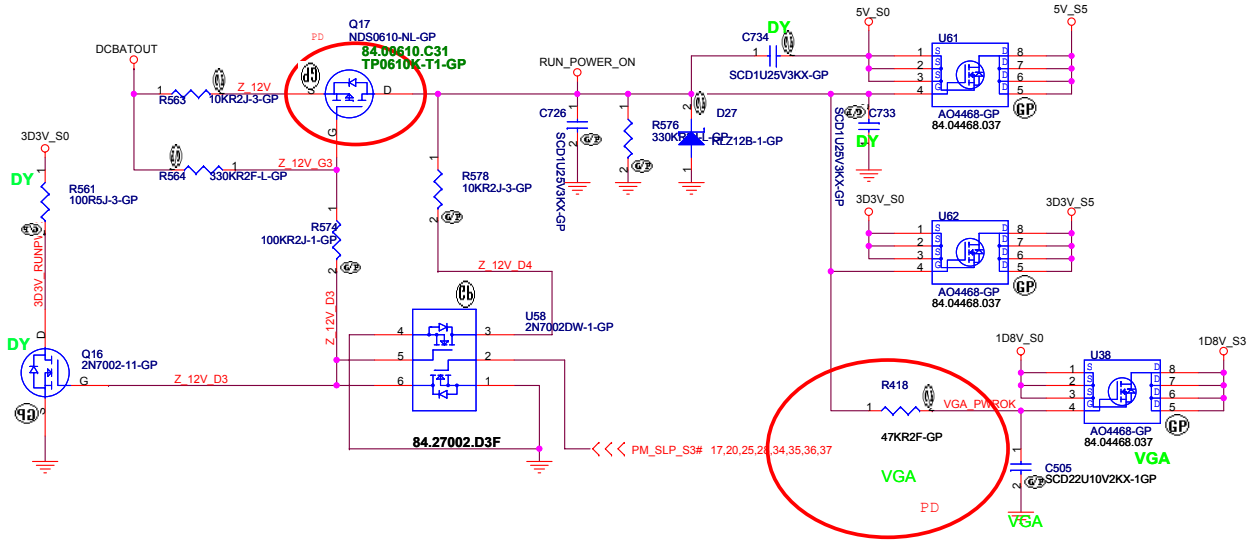
Date: Friday, March 14, 2008 Sheet 28 of 47


Internal Speaker
Headphone OUT
MIC IN/LINE IN
Internal MIC
PD USE 71.00269.A03
CLOSE to CODEC
cap close to pin39, pin46
U59
ALC269Q-GR-GP
SPK1
SPK2
HP1
PHONE-JK241-GP-U
ETY-CON2-45-GP
20.F0984.002
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ALC269 / AUDIO JACK
D45/D46
Date: Friday, March 14, 2008
Sheet 29 of 47

Aux Power 3D3V_AUX_S5

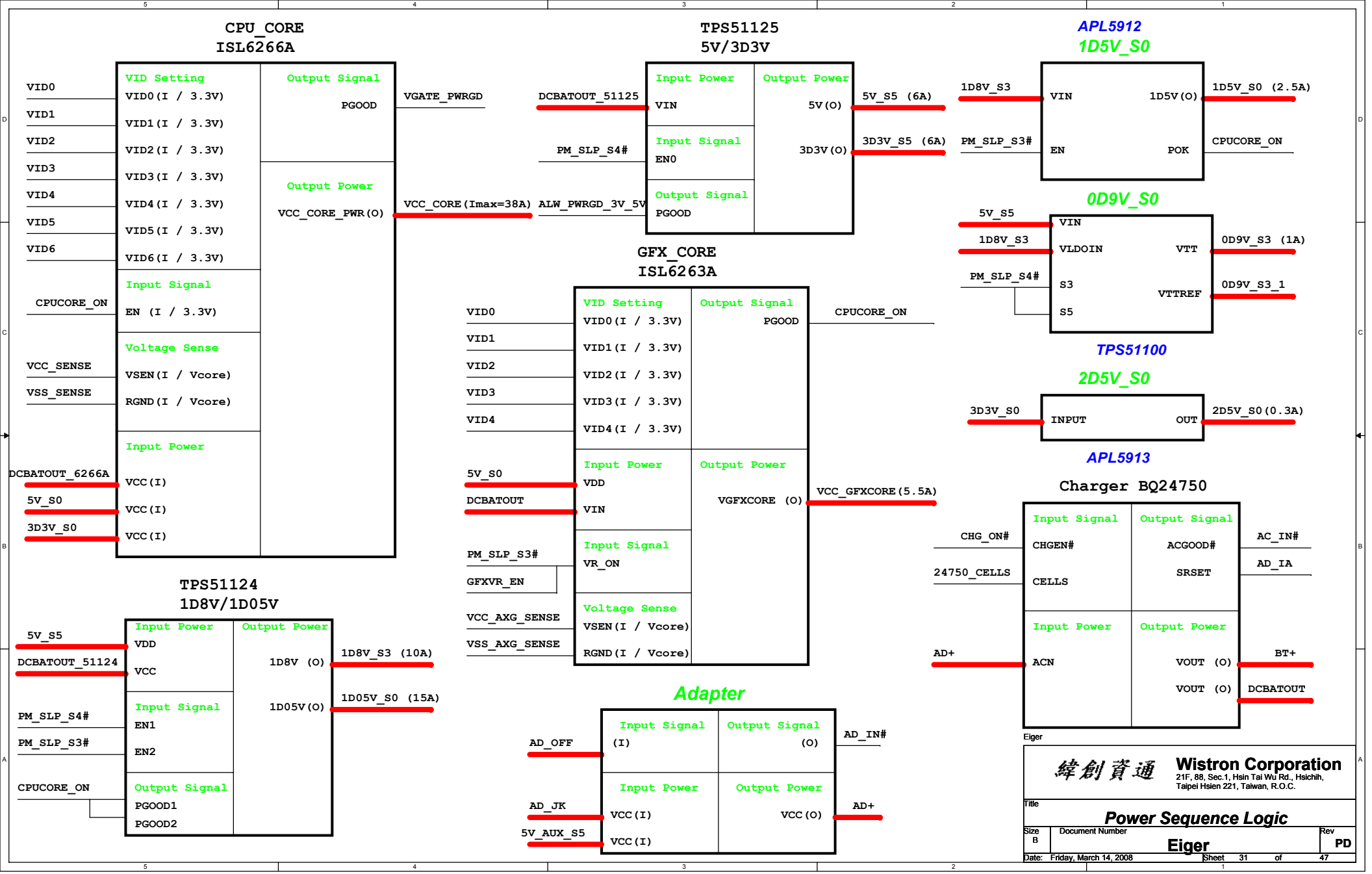


Run Power



zzzz

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RUN POWER and 3D3V_AUX_S5***	
Size	Document Number **D45/D46**	Rev PD
Date: Friday, March 14, 2008	Sheet 30 of 47	



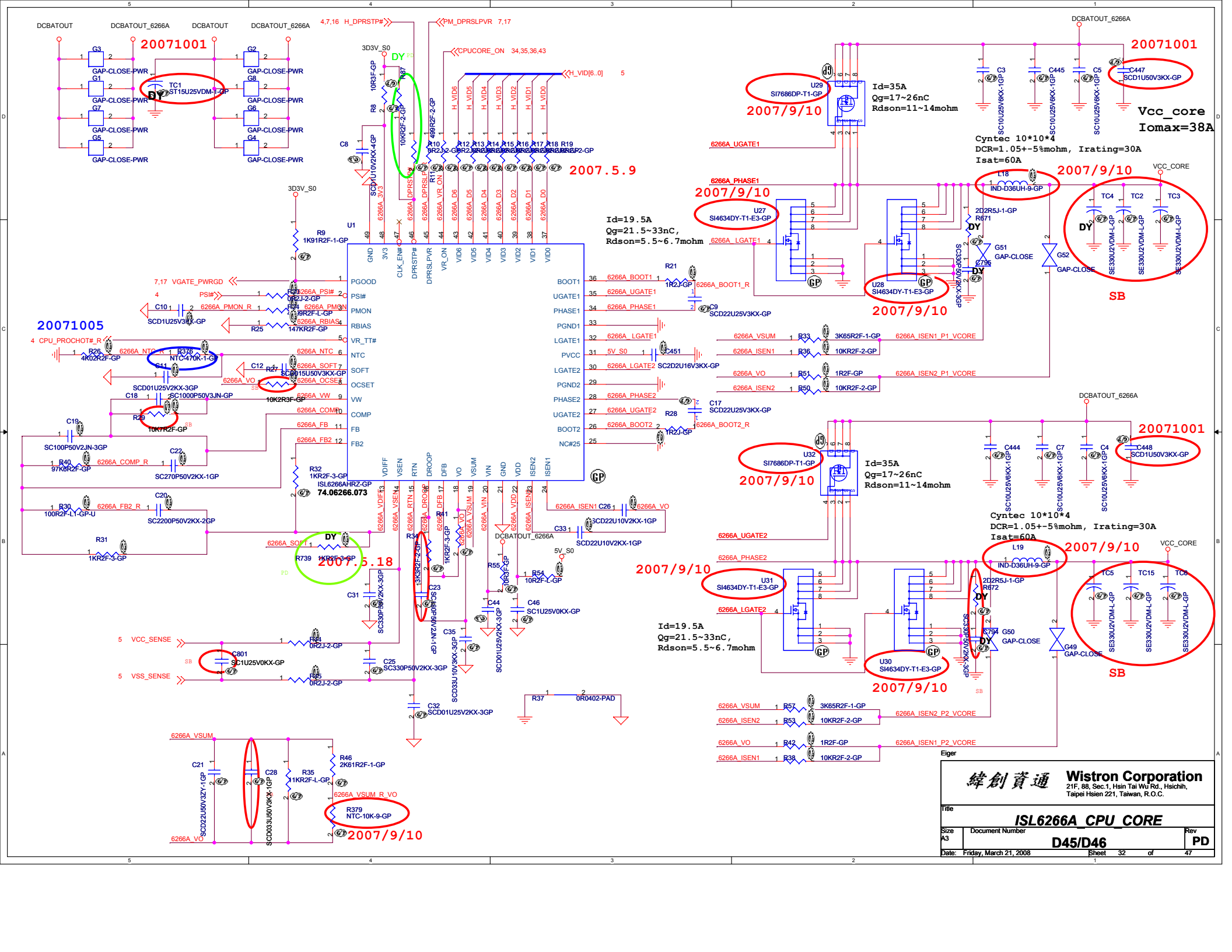
Eiger

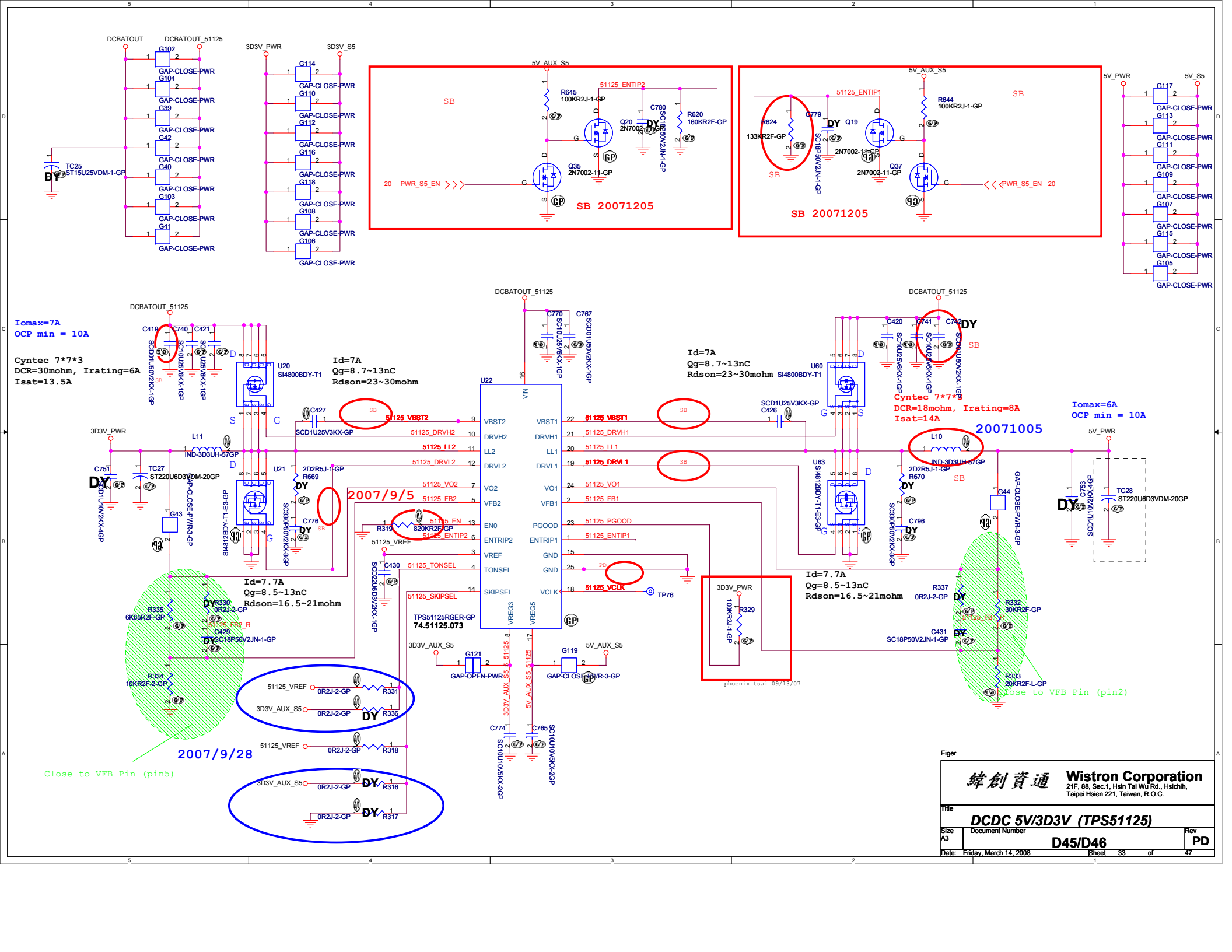
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

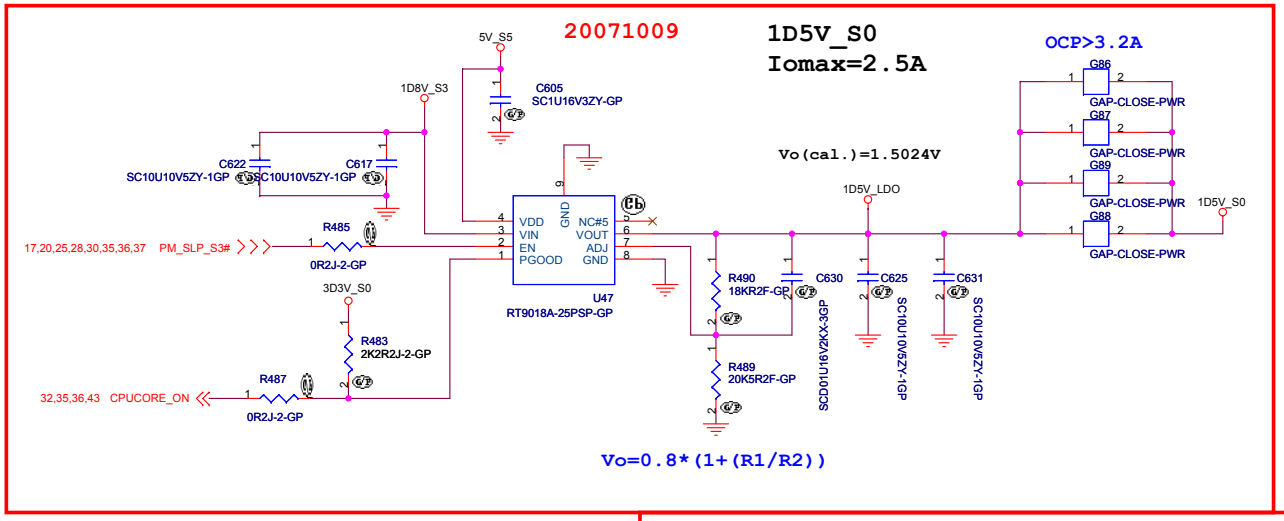
Title: **Power Sequence Logic**

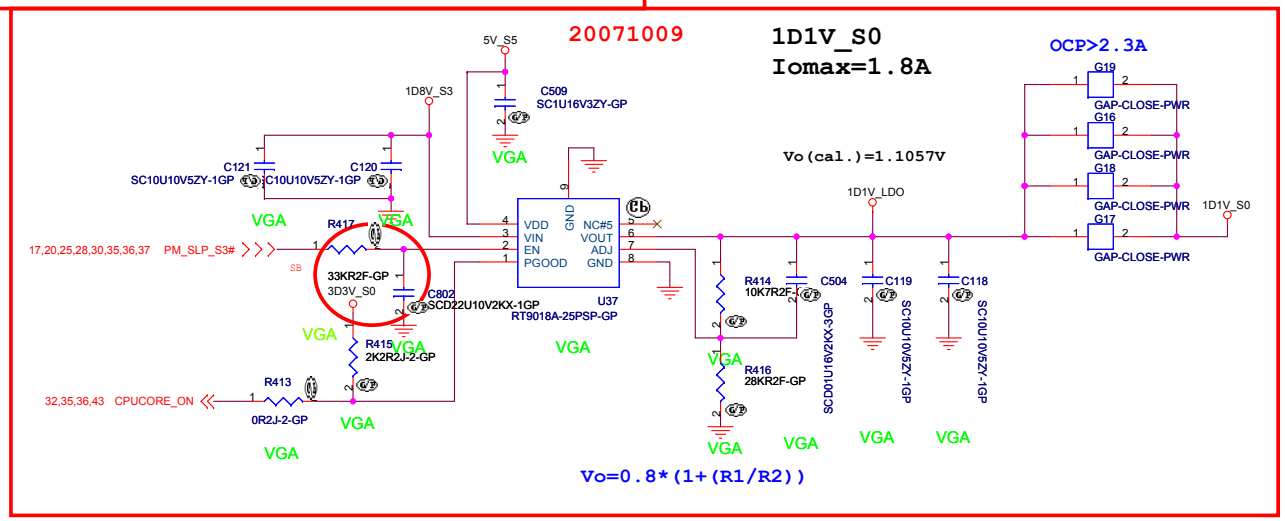
Size	Document Number	Rev
B	Eiger	PD

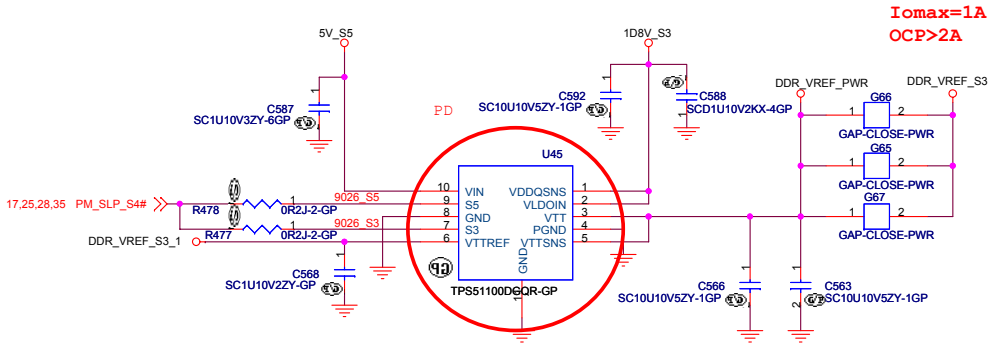
Date: Friday, March 14, 2008 Sheet 31 of 47


DCBATOUT
DCBATOUT_6266A
20071001
GAP-CLOSE-PWR
TC1
ST15U25VDM-1-GP
4,7,16 H_DPRSTP#
PM_DPRSLPVR 7,17
CPUCORE_ON 34,35,36,43
H_VID[6..0] 5
3D3V_S0
DY
2007.5.9
U1
ISL6266AHRZ-GP
74.06266.073
20071005
7,17 VGATE_PWRGD
4 PSI#
4 CPU_PROCHOT#_R
5 VCC_SENSE
5 VSS_SENSE
2007.5.18
U29
SI7686DP-T1-GP
U27
SI4634DY-T1-E3-GP
U28
SI4634DY-T1-E3-GP
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
2007/9/10
SB
U32
SI7686DP-T1-GP
U31
SI4634DY-T1-E3-GP
U30
SI4634DY-T1-E3-GP
Eiger
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number
D45/D46
Rev PD
Date: Friday, March 21, 2008
Sheet 32 of 47


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
SB
SB 20071205
SB 20071205
Iomax=7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
Iomax=6A
OCP min = 10A
20071005
2007/9/5
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
2007/9/28
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
TPS51125RGER-GP
74.51125.073
phoenix tsai 09/13/07
Eiger
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
D45/D46
PD
Friday, March 14, 2008
33
47



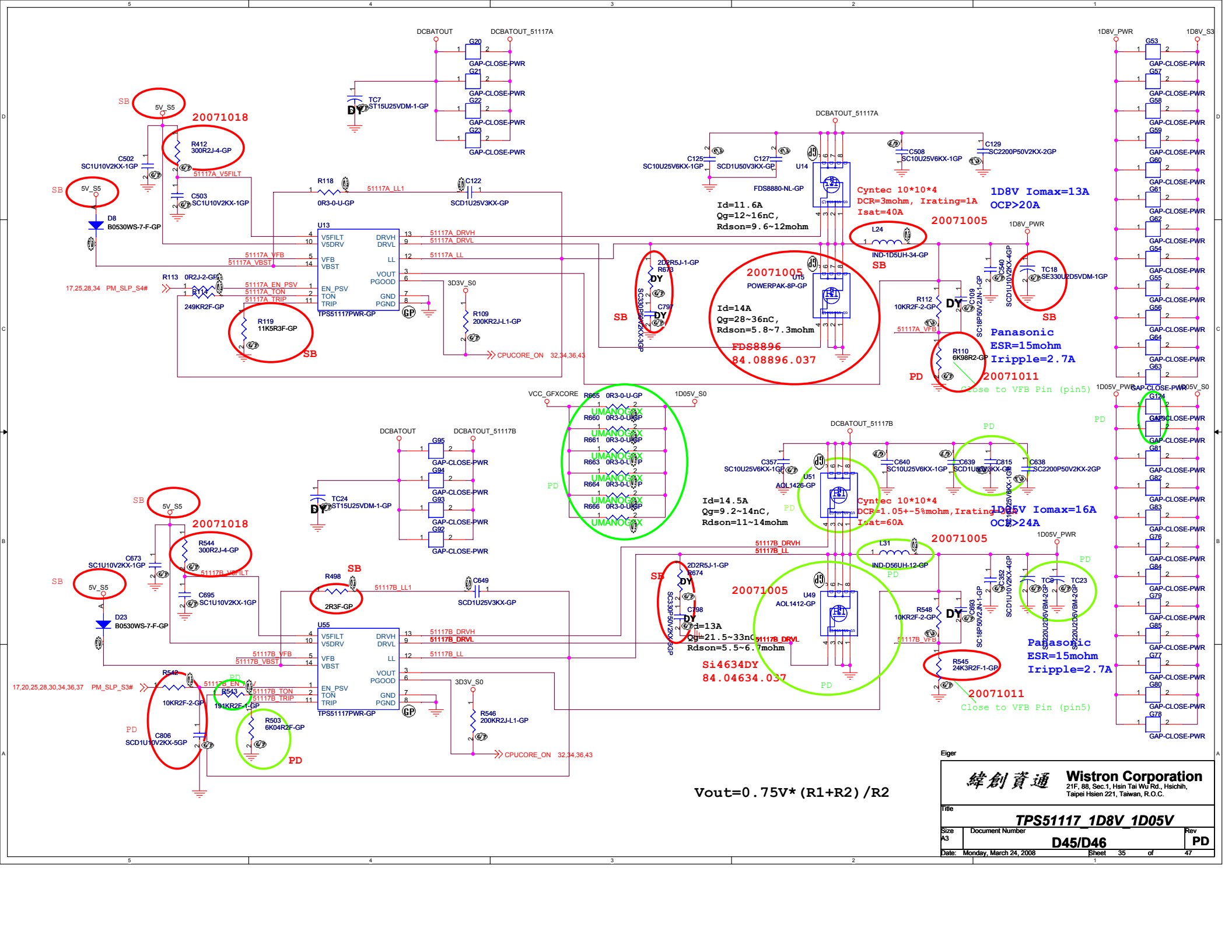


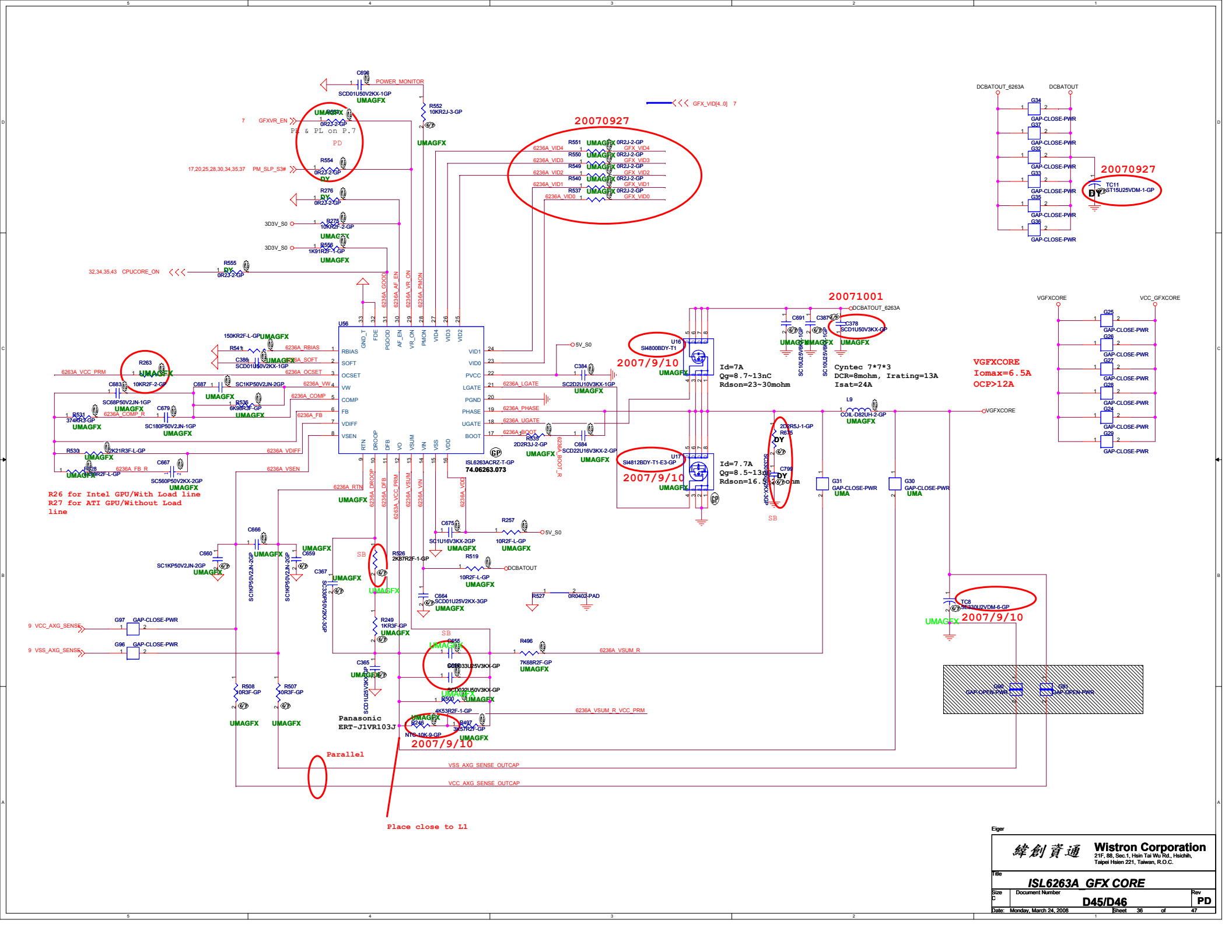


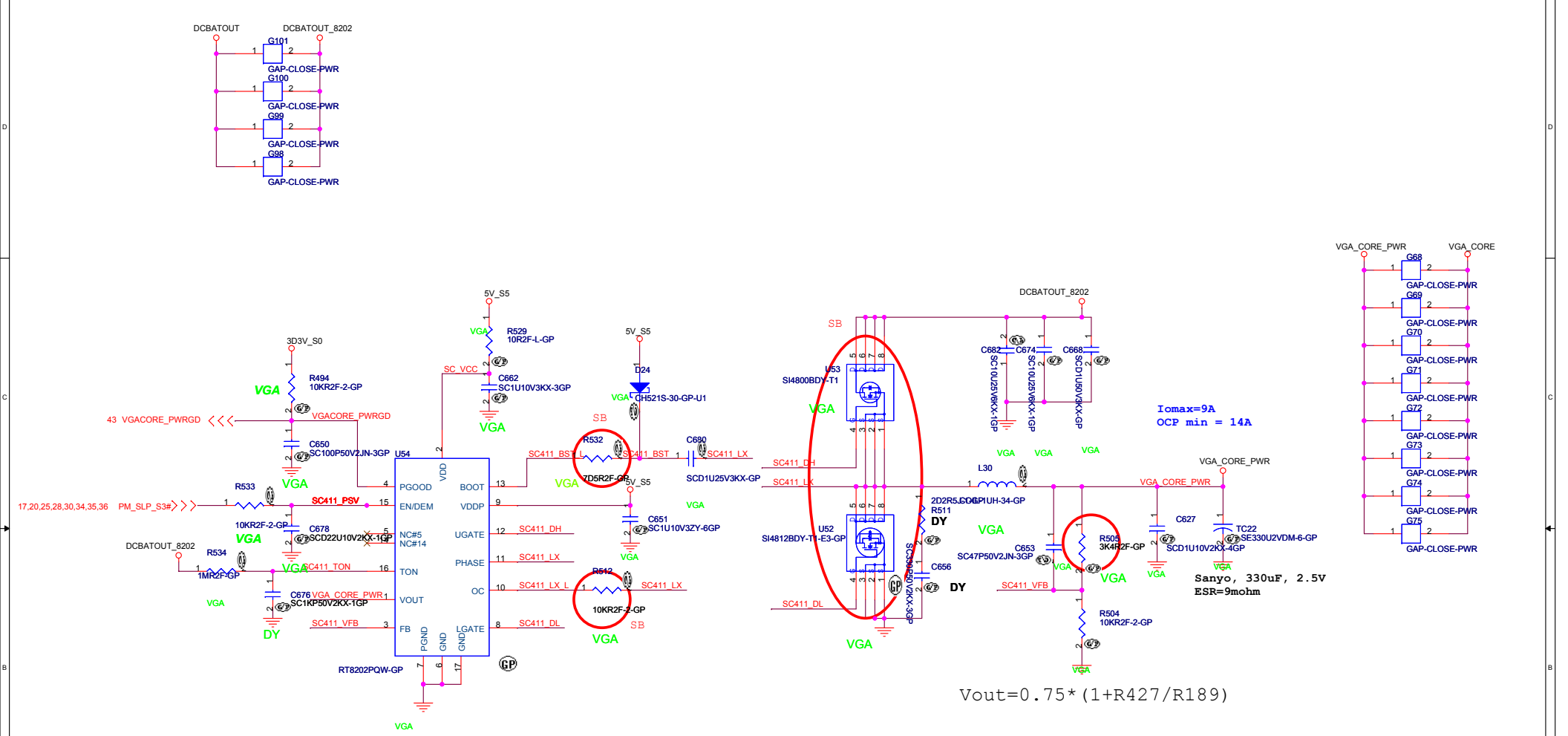
Eiger

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D5V & 0D9V	
Size A3	Document Number D45/D46	Rev PD
Date: Friday, March 14, 2008	Sheet 34 of 47	


DCBATOUT
DCBATOUT_51117A
G20
G21
G22
G23
GAP-CLOSE-PWR
TC7
ST15U25VDM-1-GP
DY
SB
5V_S5
20071018
R412
300R2J-4-GP
C502
SC1U10V2KX-1GP
51117A_V5FILT
C503
SC1U10V2KX-1GP
R118
0R3-0-U-GP
51117A_LL1
C122
SCD1U25V3KX-GP
U13
V5FILT
V5DRV
VFB
VBST
EN_PSV
TON
TRIP
DRVH
DRVL
LL
VOUT
PGOOD
GND
PGND
TPS51117PWR-GP
51117A_DRVH
51117A_DRVL
51117A_LL
51117A_VFB
51117A_VBST
51117A_EN_PSV
51117A_TON
51117A_TRIP
3D3V_S0
R113
0R2J-2-GP
17,25,28,34 PM_SLP_S4#
R114
249KR2F-GP
R119
11K5R3F-GP
R109
200KR2J-L1-GP
CPUCORE_ON 32,34,36,43
D8
B0530WS-7-F-GP
DCBATOUT_51117A
C125
SC10U25V6KX-1GP
C127
SCD1U50V3KX-GP
U14
FDS8880-NL-GP
C508
SC10U25V6KX-1GP
C129
SC2200P50V2KX-2GP
Id=11.6A
Qg=12~16nC,
Rdson=9.6~12mohm
Cyntec 10*10*4
DCR=3mohm, Irating=1A
Isat=40A
1D8V Iomax=13A
OCP>20A
20071005
L24
IND-1D5UH-34-GP
1D8V_PWR
C540
SCD1U10V2KX-4GP
C109
SC18P50V2JN-1-GP
TC18
SE330U2D5VDM-1GP
Panasonic
ESR=15mohm
Iripple=2.7A
2D2R5J-1-GP
R673
C797
SC330P50V2KX-3GP
U15
POWERPAK-8P-GP
Id=14A
Qg=28~36nC,
Rdson=5.8~7.3mohm
FDS8896
84.08896.037
R112
10KR2F-2-GP
R110
6K98R2-GP
20071011
Close to VFB Pin (pin5)
PD
VCC_GFXCORE
1D05V_S0
R665
R660
R661
R663
R664
R666
0R3-0-U-GP
UMANOCAX
1D05V_PWR
G53
G57
G58
G59
G60
G61
G62
G54
G55
G56
G64
G63
G124
G81
G82
G83
G76
G84
G79
G85
G77
G80
G78
DCBATOUT
DCBATOUT_51117B
G95
G94
G93
G92
TC24
ST15U25VDM-1-GP
C673
SC1U10V2KX-1GP
R544
300R2J-4-GP
51117B_V5FILT
C695
SC1U10V2KX-1GP
D23
B0530WS-7-F-GP
R498
2R3F-GP
51117B_LL1
C649
SCD1U25V3KX-GP
U55
51117B_DRVH
51117B_DRVL
51117B_LL
51117B_VFB
51117B_VBST
51117B_EN_PSV
51117B_TON
51117B_TRIP
17,20,25,28,30,34,36,37 PM_SLP_S3#
R542
10KR2F-2-GP
R543
191KR2F-GP
R503
6K04R2F-GP
C806
SCD1U10V2KX-5GP
R546
200KR2J-L1-GP
CPUCORE_ON 32,34,36,43
DCBATOUT_51117B
C357
SC10U25V6KX-1GP
U51
AOL1426-GP
C640
SC10U25V6KX-1GP
C639
SCD1U50V3KX-GP
C815
SC10U25V6KX-1GP
C638
SC2200P50V2KX-2GP
Id=14.5A
Qg=9.2~14nC,
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=20A
Isat=60A
1D05V Iomax=16A
OCP>24A
20071005
L31
IND-D56UH-12-GP
1D05V_PWR
C352
SCD1U10V2KX-4GP
C863
SC18P50V2JN-1-GP
TC8
TC23
SP220U2D5VBM-2GP
Panasonic
ESR=15mohm
Iripple=2.7A
2D2R5J-1-GP
R674
C798
SC330P50V2KX-3GP
U49
AOL1412-GP
Id=13A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Si4634DY
84.04634.037
R548
10KR2F-2-GP
R545
24K3R2F-1-GP
20071011
Close to VFB Pin (pin5)
Vout=0.75V*(R1+R2)/R2
Eiger
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51117_1D8V_1D05V
Size
A3
Document Number
D45/D46
Rev
PD
Date: Monday, March 24, 2008
Sheet 35 of 47


U56
ISL6263ACRZ-T-GP
74.06263.073
20070927
20071001
2007/9/10
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cytnec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7.7A
Qg=8.5~13nC
Rdson=16.2mohm
VGFXCORE
Iomax=6.5A
OCP>12A
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
Parallel
Place close to L1
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
D45/D46
Monday, March 24, 2008



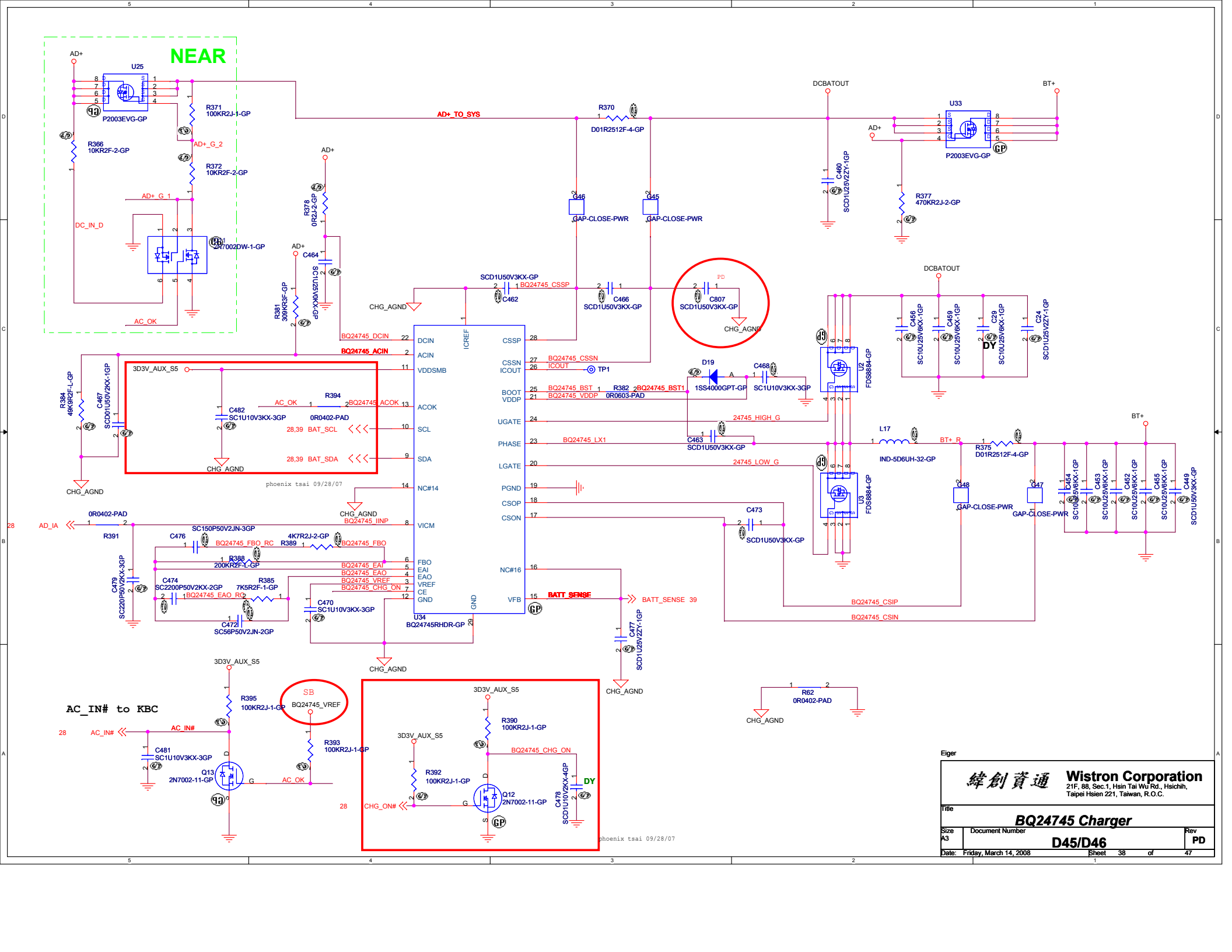
Eiger

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA_CORE_S0 (UMA)**

Size	Document Number	Rev
A3	D45/D46	PD

Date: Friday, March 14, 2008 Sheet 37 of 47



Eiger

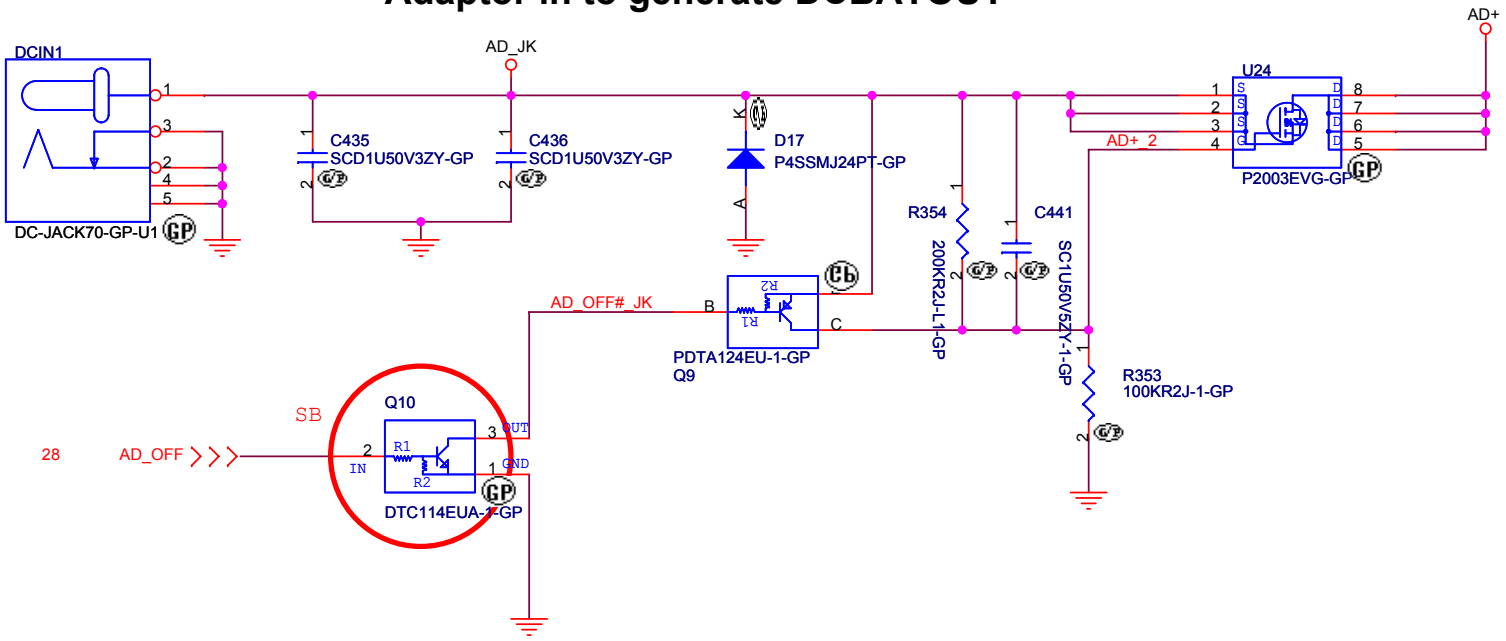
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

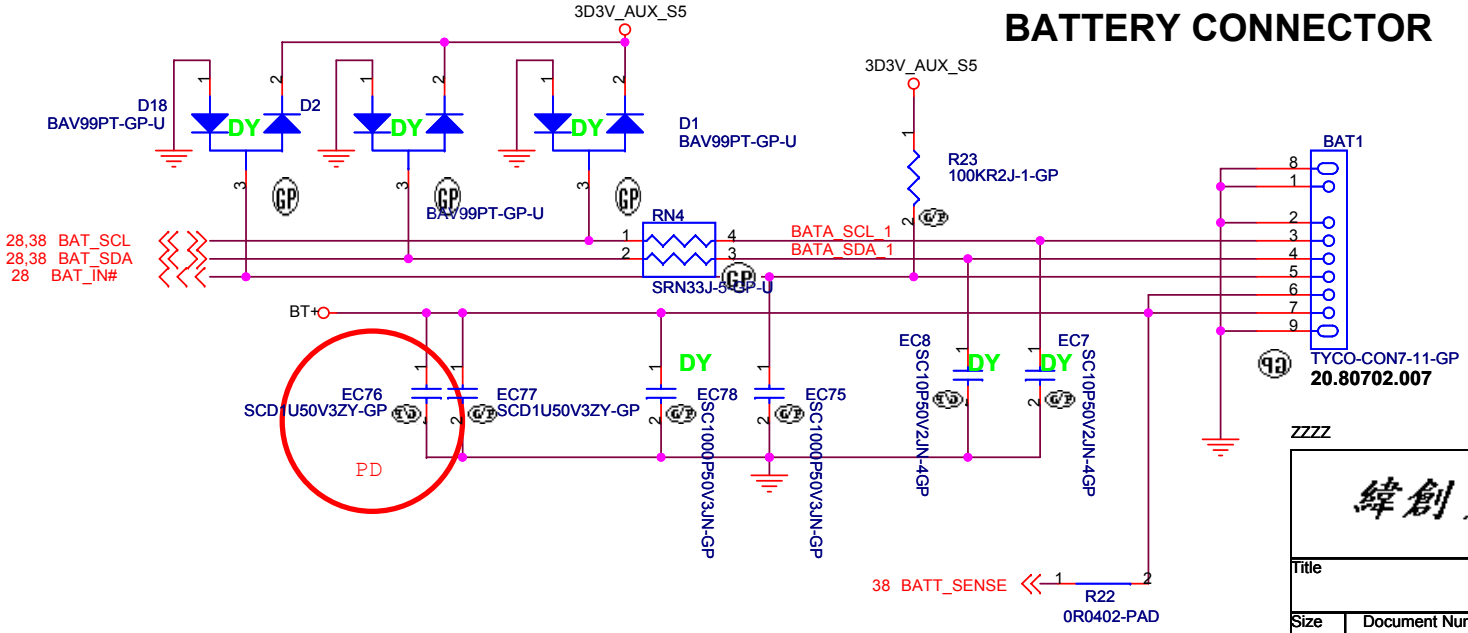
Size	Document Number	Rev
A3	D45/D46	PD

Date: Friday, March 14, 2008 Sheet 38 of 47

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

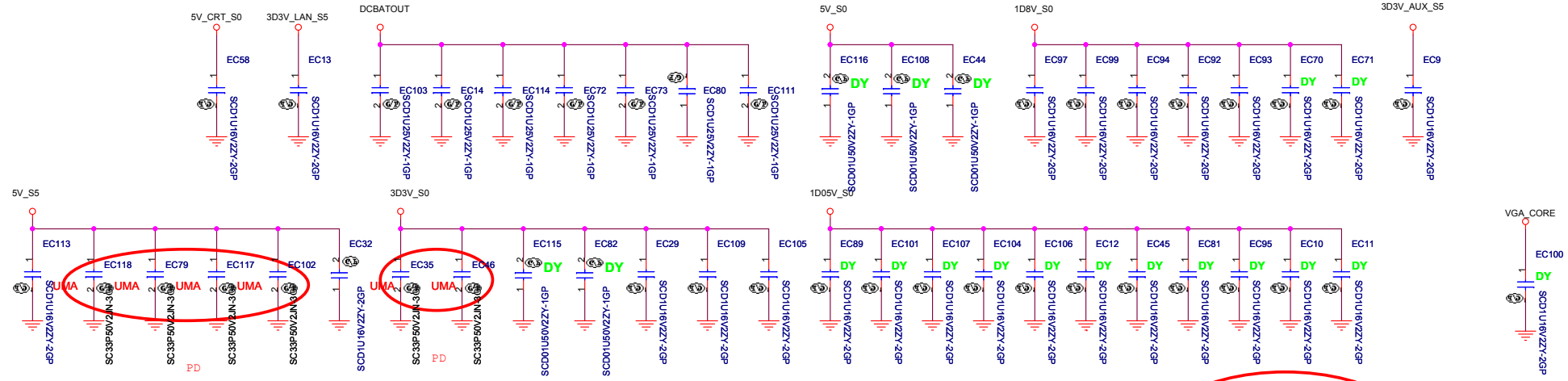


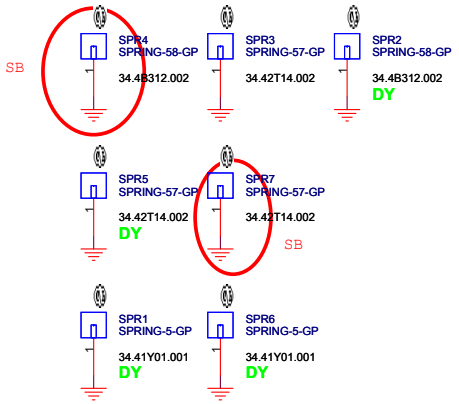
ZZZZ

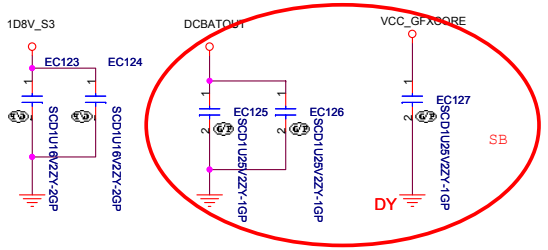
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: D45/D46	Rev: PD
Date: Monday, March 24, 2008	Sheet 39 of 47	

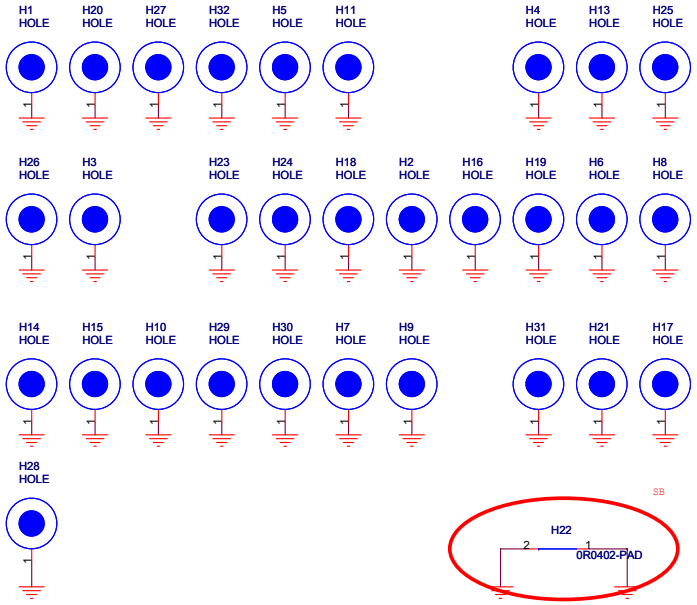
EMI Caps

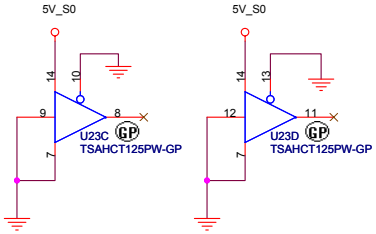




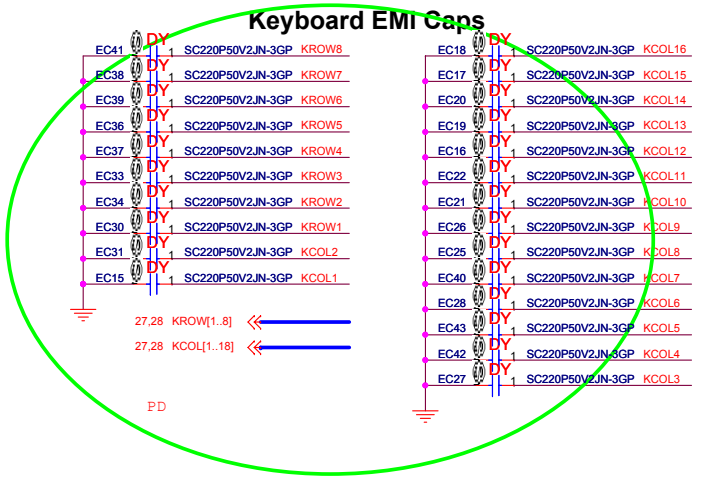


Holes





Keyboard EMI Caps

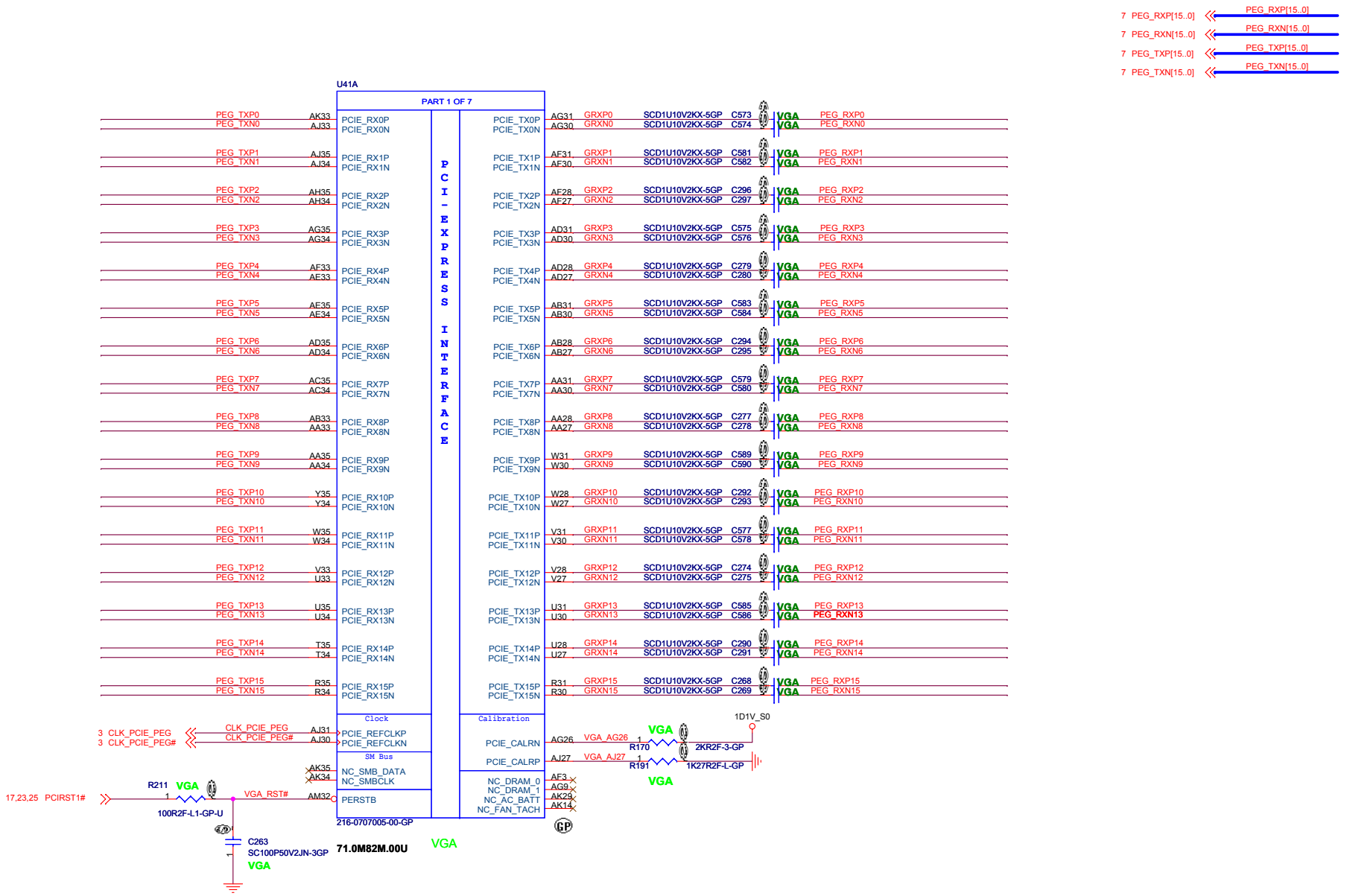


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

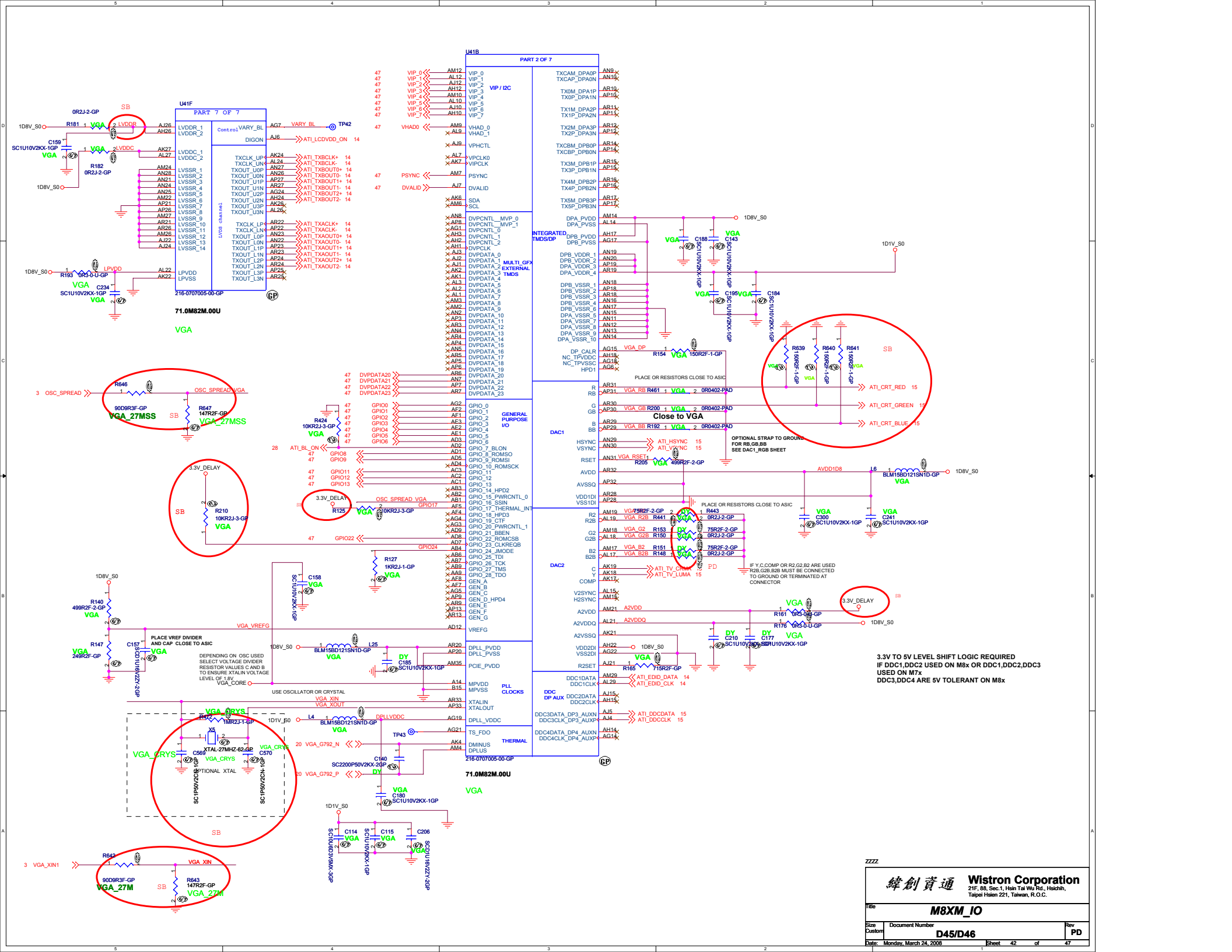
Size | Document Number: **D45/D46** | Rev: **PD**

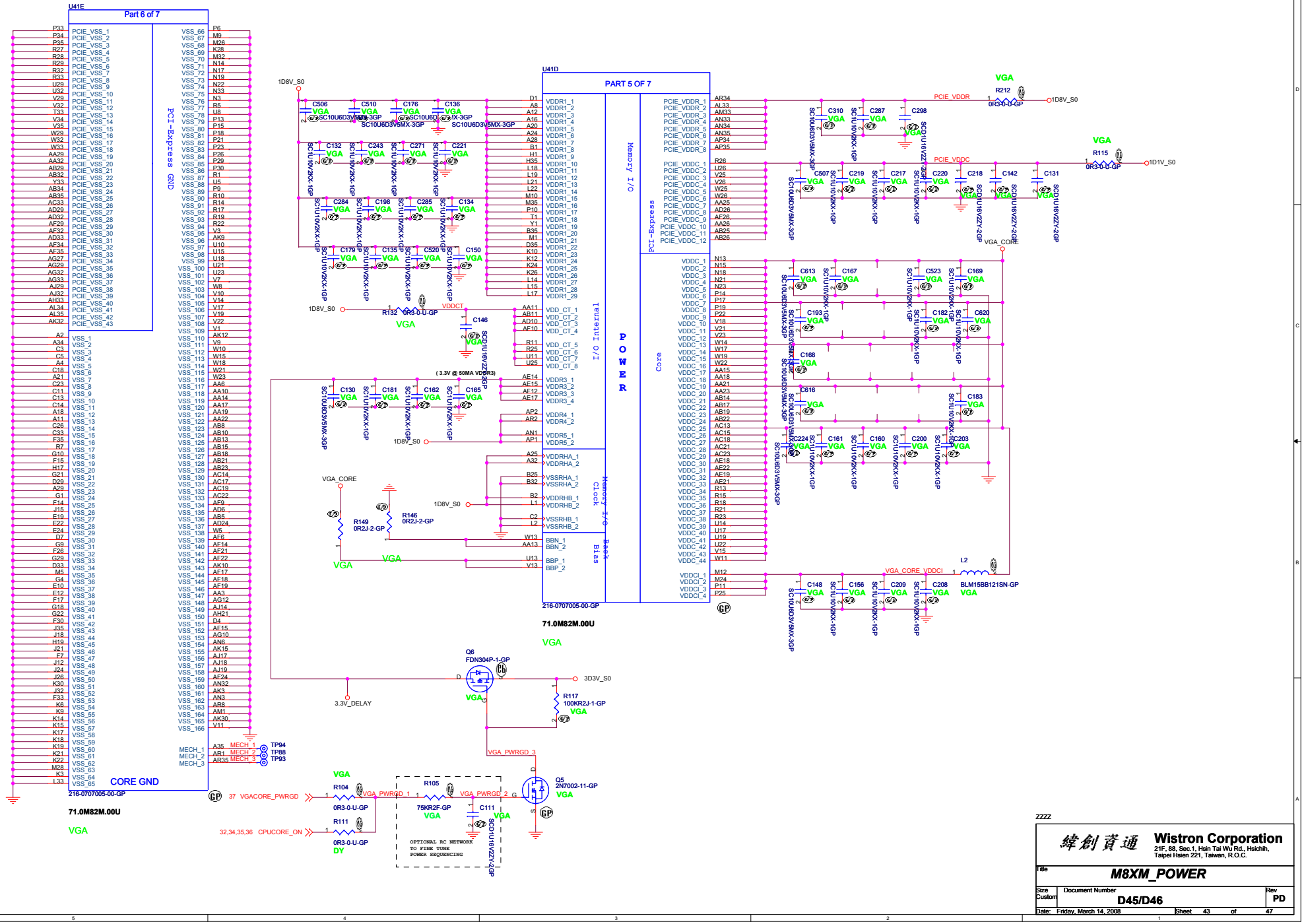
Date: Monday, March 17, 2008 | Sheet 40 of 47

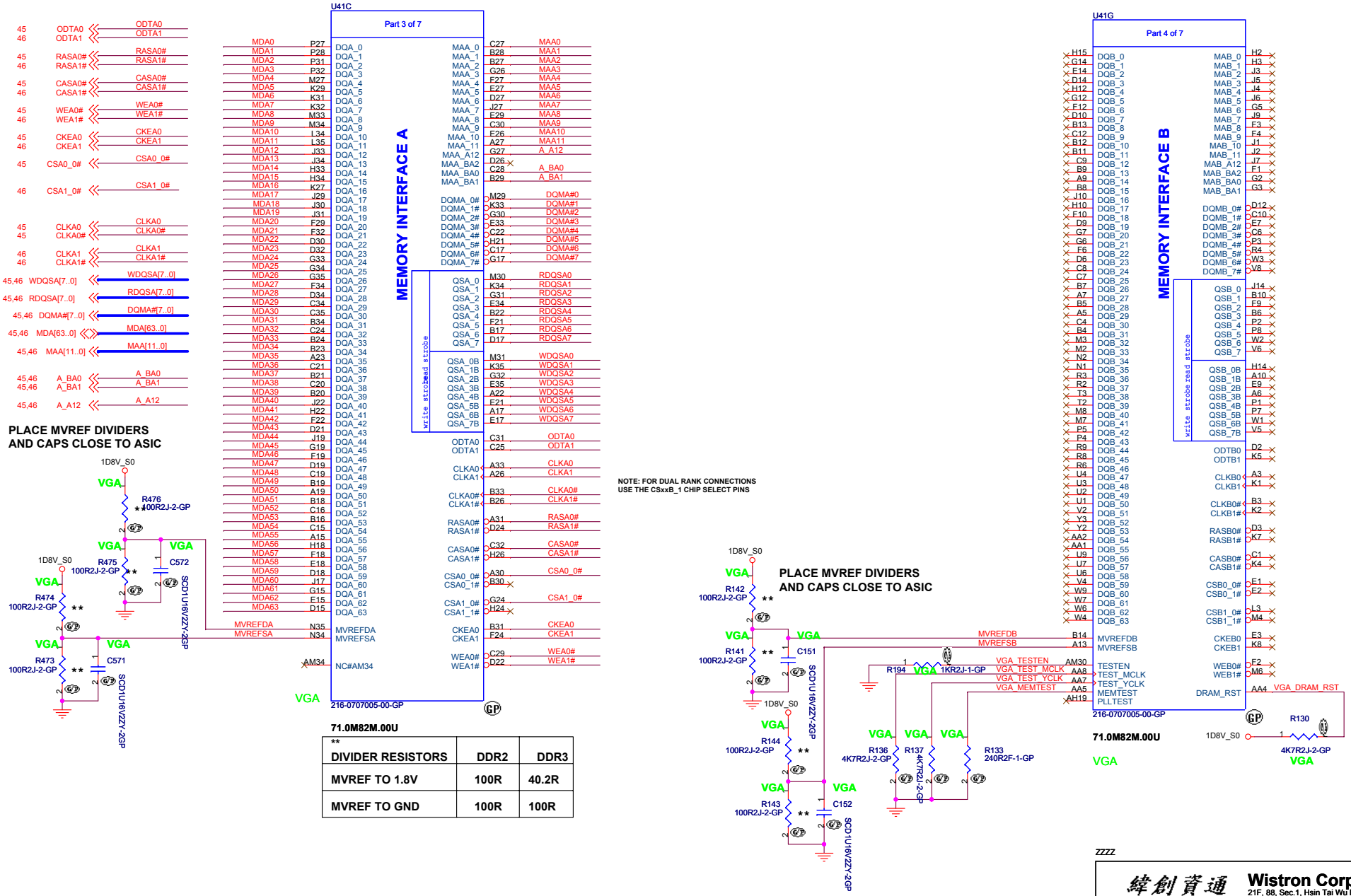


ZZZZ

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M8XM_PCIE***	
Size	Document Number **D45/D46**	Rev **PD**
Date: Friday, March 14, 2008	Sheet 41 of 47	


U41B
PART 2 OF 7
U41F
PART 7 OF 7
VIP / I2C
INTEGRATED TMDS/DP
MULTI_GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
DAC1
DAC2
DDC DP AUX
PLL CLOCKS
THERMAL
216-0707005-00-GP
71.0M82M.00U
VGA
Close to VGA
PLACE OR RESISTORS CLOSE TO ASIC
OPTIONAL STRAP TO GROUND FOR RB,GB,BB SEE DAC1_RGB SHEET
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC
DEPENDING ON OSC USED SELECT VOLTAGE DIVIDER RESISTOR VALUES C AND B TO ENSURE XTALIN VOLTAGE LEVEL OF 1.8V
USE OSCILLATOR OR CRYSTAL
IF Y,C,COMP OR R2,G2,B2 ARE USED R2B,G2B,B2B MUST BE CONNECTED TO GROUND OR TERMINATED AT CONNECTOR
3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED
IF DDC1,DDC2 USED ON M8x OR DDC1,DDC2,DDC3 USED ON M7x
DDC3,DDC4 ARE 5V TOLERANT ON M8x
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
M8XM_IO
D45/D46
PD
Monday, March 24, 2008
42 of 47


U41E
Part 6 of 7
PCI_Express GND
CORE GND
216-0707005-00-GP
71.0M82M.00U
VGA
U41D
PART 5 OF 7
Memory I/O
I/O Internal
POWER
Core
Clock
Memory I/O Bias
216-0707005-00-GP
71.0M82M.00U
VGA
1D8V_S0
1D1V_S0
3D3V_S0
VGA_CORE
PCIE_VDDR
PCIE_VDDC
VGA_CORE_VDDCI
VDDCT
3.3V_DELAY
(3.3V @ 50MA VDDR3)
Q6
FDN304P-1-GP
Q5
2N7002-11-GP
R212
0R3-0-U-GP
R115
0R3-0-U-GP
R132
0R3-0-U-GP
R146
0R2J-2-GP
R149
0R2J-2-GP
R117
100KR2J-1-GP
R104
0R3-0-U-GP
R111
0R3-0-U-GP
R105
75KR2F-GP
L2
BLM15BB121SN-GP
37 VGACORE_PWRGD
32,34,35,36 CPUCORE_ON
VGA_PWRGD_1
VGA_PWRGD_2
VGA_PWRGD_3
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING
DY
TP94
TP88
TP93
zzzz
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
M8XM_POWER
Size
Custom
Document Number
D45/D46
Rev
PD
Date: Friday, March 14, 2008
Sheet 43 of 47


U41C
Part 3 of 7
MEMORY INTERFACE A
DQA_0
DQA_1
DQA_2
DQA_3
DQA_4
DQA_5
DQA_6
DQA_7
DQA_8
DQA_9
DQA_10
DQA_11
DQA_12
DQA_13
DQA_14
DQA_15
DQA_16
DQA_17
DQA_18
DQA_19
DQA_20
DQA_21
DQA_22
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DQA_42
DQA_43
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DQA_51
DQA_52
DQA_53
DQA_54
DQA_55
DQA_56
DQA_57
DQA_58
DQA_59
DQA_60
DQA_61
DQA_62
DQA_63
MAA_0
MAA_1
MAA_2
MAA_3
MAA_4
MAA_5
MAA_6
MAA_7
MAA_8
MAA_9
MAA_10
MAA_11
MAA_A12
MAA_BA2
MAA_BA0
MAA_BA1
DQMA_0#
DQMA_1#
DQMA_2#
DQMA_3#
DQMA_4#
DQMA_5#
DQMA_6#
DQMA_7#
QSA_0
QSA_1
QSA_2
QSA_3
QSA_4
QSA_5
QSA_6
QSA_7
QSA_0B
QSA_1B
QSA_2B
QSA_3B
QSA_4B
QSA_5B
QSA_6B
QSA_7B
ODTA0
ODTA1
CLKA0
CLKA1
CLKA0#
CLKA1#
RASA0#
RASA1#
CASA0#
CASA1#
CSA0_0#
CSA1_0#
CKEA0
CKEA1
WEA0#
WEA1#
A_BA0
A_BA1
A_A12
MVREFDA
MVREFSA
NC#AM34
write strobe
read strobe
216-0707005-00-GP
71.0M82M.00U
MDA0
MDA1
MDA2
MDA3
MDA4
MDA5
MDA6
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MAA4
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MAA6
MAA7
MAA8
MAA9
MAA10
MAA11
A_A12
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A_BA1
DQMA#0
DQMA#1
DQMA#2
DQMA#3
DQMA#4
DQMA#5
DQMA#6
DQMA#7
RDQSA0
RDQSA1
RDQSA2
RDQSA3
RDQSA4
RDQSA5
RDQSA6
RDQSA7
WDQSA0
WDQSA1
WDQSA2
WDQSA3
WDQSA4
WDQSA5
WDQSA6
WDQSA7
ODTA0
ODTA1
CLKA0
CLKA1
CLKA0#
CLKA1#
RASA0#
RASA1#
CASA0#
CASA1#
CSA0_0#
CSA1_0#
CKEA0
CKEA1
WEA0#
WEA1#
A_BA0
A_BA1
A_A12
MVREFDA
MVREFSA
45 ODTA0
46 ODTA1
45 RASA0#
46 RASA1#
45 CASA0#
46 CASA1#
45 WEA0#
46 WEA1#
45 CKEA0
46 CKEA1
45 CSA0_0#
46 CSA1_0#
45 CLKA0
45 CLKA0#
46 CLKA1
46 CLKA1#
45,46 WDQSA[7..0]
45,46 RDQSA[7..0]
45,46 DQMA#[7..0]
45,46 MDA[63..0]
45,46 MAA[11..0]
45,46 A_BA0
45,46 A_BA1
45,46 A_A12
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
1D8V_S0
VGA
R476
100R2J-2-GP
R475
100R2J-2-GP
C572
R474
100R2J-2-GP
R473
100R2J-2-GP
C571
SCD1U16V2ZY-2GP
NOTE: FOR DUAL RANK CONNECTIONS
USE THE CSxxB_1 CHIP SELECT PINS
R142
100R2J-2-GP
R141
100R2J-2-GP
C151
R144
100R2J-2-GP
R143
100R2J-2-GP
C152
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
MVREFDB
MVREFSB
VGA_TESTEN
VGA_TEST_MCLK
VGA_TEST_YCLK
VGA_MEMTEST
R194
1KR2J-1-GP
R136
4K7R2J-2-GP
R137
4K7R2J-2-GP
R133
240R2F-1-GP
U41G
Part 4 of 7
MEMORY INTERFACE B
DQB_0
DQB_1
DQB_2
DQB_3
DQB_4
DQB_5
DQB_6
DQB_7
DQB_8
DQB_9
DQB_10
DQB_11
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DQB_60
DQB_61
DQB_62
DQB_63
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MAB_2
MAB_3
MAB_4
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MAB_9
MAB_10
MAB_11
MAB_A12
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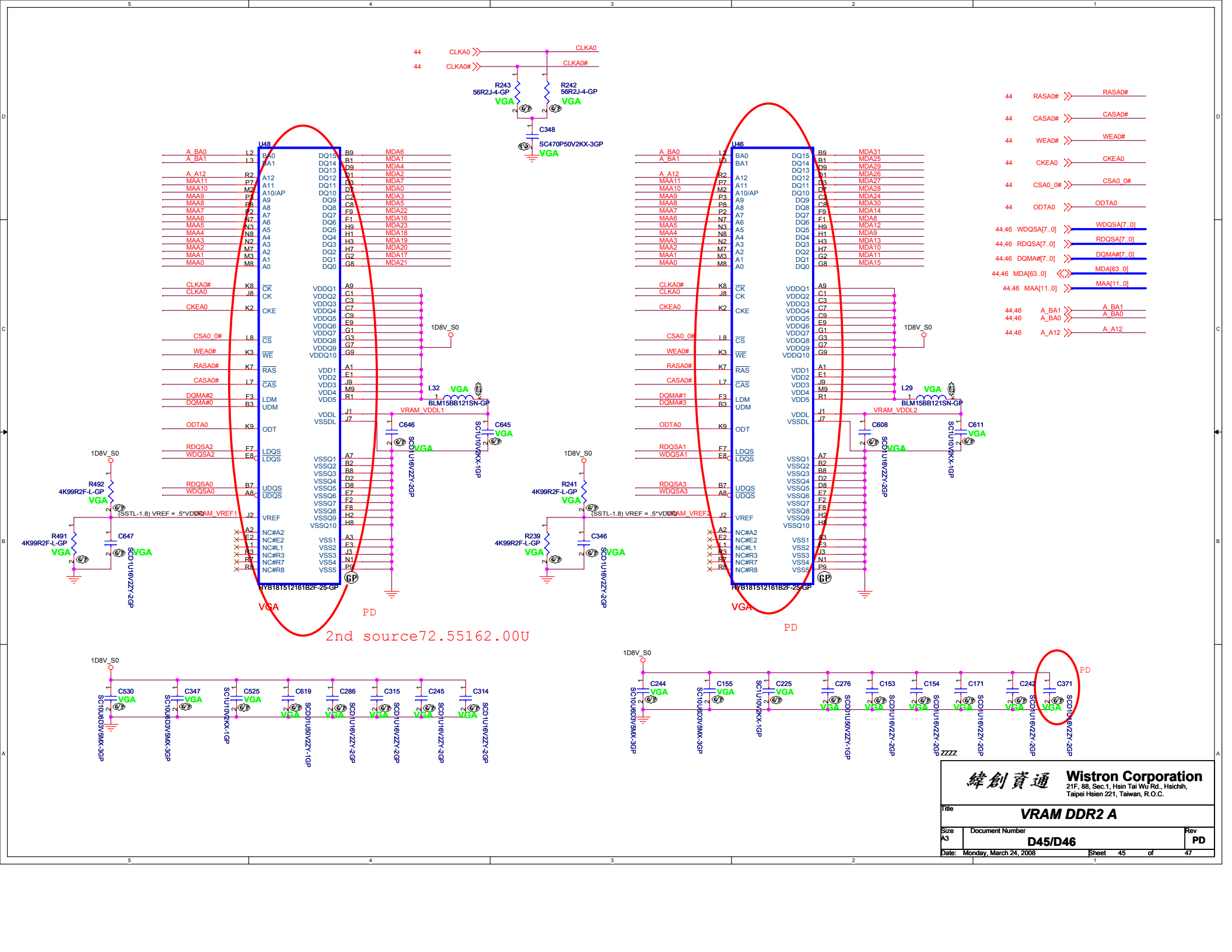
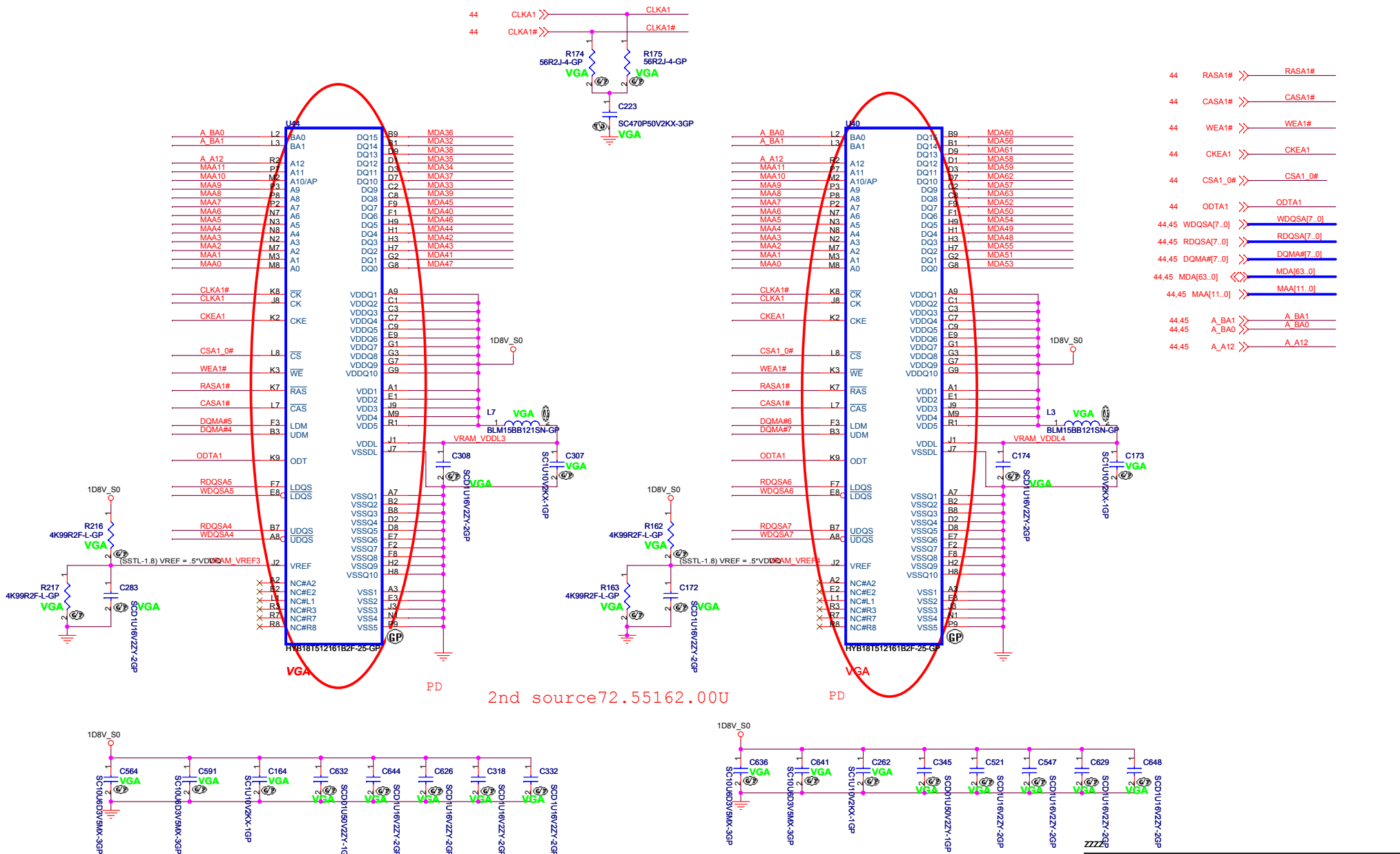
MAB_BA0
MAB_BA1
DQMB_0#
DQMB_1#
DQMB_2#
DQMB_3#
DQMB_4#
DQMB_5#
DQMB_6#
DQMB_7#
QSB_0
QSB_1
QSB_2
QSB_3
QSB_4
QSB_5
QSB_6
QSB_7
QSB_0B
QSB_1B
QSB_2B
QSB_3B
QSB_4B
QSB_5B
QSB_6B
QSB_7B
ODTB0
ODTB1
CLKB0
CLKB1
CLKB0#
CLKB1#
RASB0#
RASB1#
CASB0#
CASB1#
CSB0_0#
CSB0_1#
CSB1_0#
CSB1_1#
CKEB0
CKEB1
WEB0#
WEB1#
TESTEN
TEST_MCLK
TEST_YCLK
MEMTEST
PLLTEST
DRAM_RST
VGA_DRAM_RST
R130
4K7R2J-2-GP
216-0707005-00-GP
71.0M82M.00U
** DIVIDER RESISTORS DDR2 DDR3
MVREF TO 1.8V 100R 40.2R
MVREF TO GND 100R 100R
ZZZZ
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M8XM_MEMORY
Size A3
Document Number D45/D46
Rev PD
Date: Friday, March 14, 2008
Sheet 44 of 47

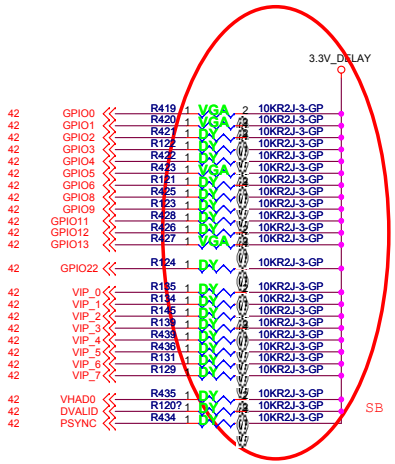

U48
U46
HY5PS121621BF-25-GP
R243 56R2J-4-GP VGA
R242 56R2J-4-GP VGA
C348 SC470P50V2KX-3GP VGA
CLKA0
CLKA0#
1D8V_S0
L32 BLM15BB121SN-GP VGA
L29 BLM15BB121SN-GP VGA
VRAM_VDDL1
VRAM_VDDL2
R492 4K99R2F-L-GP VGA
R491 4K99R2F-L-GP VGA
R241 4K99R2F-L-GP VGA
R239 4K99R2F-L-GP VGA
(SSTL-1.8) VREF = .5*VDDQ
VRAM_VREF1
VRAM_VREF2
C647 SCD1U16V2ZY-2GP VGA
C646 SCD1U16V2ZY-2GP VGA
C645 SC1U10V2KX-1GP VGA
C346 SCD1U16V2ZY-2GP VGA
C608 SCD1U16V2ZY-2GP VGA
C611 SC1U10V2KX-1GP VGA
RASA0#
CASA0#
WEA0#
CKEA0
CSA0_0#
ODTA0
WDQSA[7..0]
RDQSA[7..0]
DQMA#[7..0]
MDA[63..0]
MAA[11..0]
A_BA1
A_BA0
A_A12
PD
2nd source72.55162.00U
C530 SC10U6D3V5MX-3GP VGA
C347 SC10U6D3V5MX-3GP VGA
C525 SC1U10V2KX-1GP VGA
C619 SCD1U50V2ZY-1GP VGA
C286 SCD1U16V2ZY-2GP VGA
C315 SCD1U16V2ZY-2GP VGA
C245 SCD1U16V2ZY-2GP VGA
C314 SCD1U16V2ZY-2GP VGA
C244 SC10U6D3V5MX-3GP VGA
C155 SC10U6D3V5MX-3GP VGA
C225 SC1U10V2KX-1GP VGA
C276 SCD1U50V2ZY-1GP VGA
C153 SCD1U16V2ZY-2GP VGA
C154 SCD1U16V2ZY-2GP VGA
C171 SCD1U16V2ZY-2GP VGA
C242 SCD1U16V2ZY-2GP VGA
C371 SCD1U16V2ZY-2GP VGA
ZZZZ
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM DDR2 A
Size A3
Document Number
D45/D46
Rev PD
Date: Monday, March 24, 2008
Sheet 45 of 47

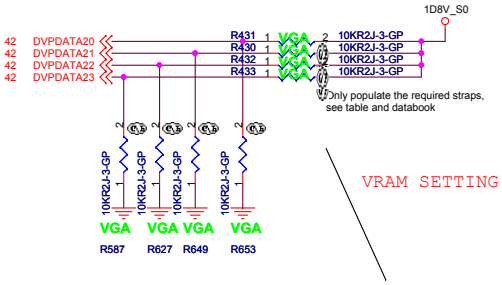


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VRAM DDR2 B***
Size A3	Document Number **D45/D46** Rev **PD**
Date: Monday, March 24, 2008	Sheet 46 of 47

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X





VRAM SETTING

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

For Hynix 上R431,R430,R432,R433 (63.10334.1DL)
Delete R587,R627,R649,R653

For Qimonda 上R431,R430,R432,R587 (63.10334.1DL)
Delete R433,R627,R649,R653

For Samsung 上R431,R430,R627,R433 (63.10334.1DL)
Delete R587,R432,R649,R653

DVPDATA20 1
DVPDATA21 1 HY5PS121621CFP-25 Hynix
DVPDATA22 1 72.51216.F0U
DVPDATA23 1

DVPDATA20 1
DVPDATA21 1 HYB18T512161B2F-25 Qimonda
DVPDATA22 1 72.18512.M0U
DVPDATA23 0

DVPDATA20 1
DVPDATA21 1 K4N51163QE-ZC25 SamSung
DVPDATA22 0 72.45116.A0U
DVPDATA23 1

DVPDATA20 1
DVPDATA21 1 H5PS5162FFR-25C
DVPDATA22 0 HYNIX
DVPDATA23 0 72.55162.00U

D45 VRAM SELECT

手動改D45 BOM U43 71.CNTIG.H0U
U57 71.ICH9M.E0U

R186,187,188,198,201,202-> 63.R0034.1DL

手動改D46 BOM U43 71.CNTIG.G0U
U57 71.ICH9M.E0U

手動改共同BOM

DM2 62.10017.G31
U49 84.04634.037
U15 84.08896.037
H29 34.4B417.001
H30 34.4B417.001
H27 34.4F403.001
H31 34.4F403.001
H7 34.4F403.001
H9 34.4F403.001
H10 34.4G501.001

U11 71.00773.00G
U64 71.00380.003
U35 62.10053.401
U7 71.08111.E03

手動改NET

DM2 62.10017.G31
U35 62.10053.401

ZZZZ

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